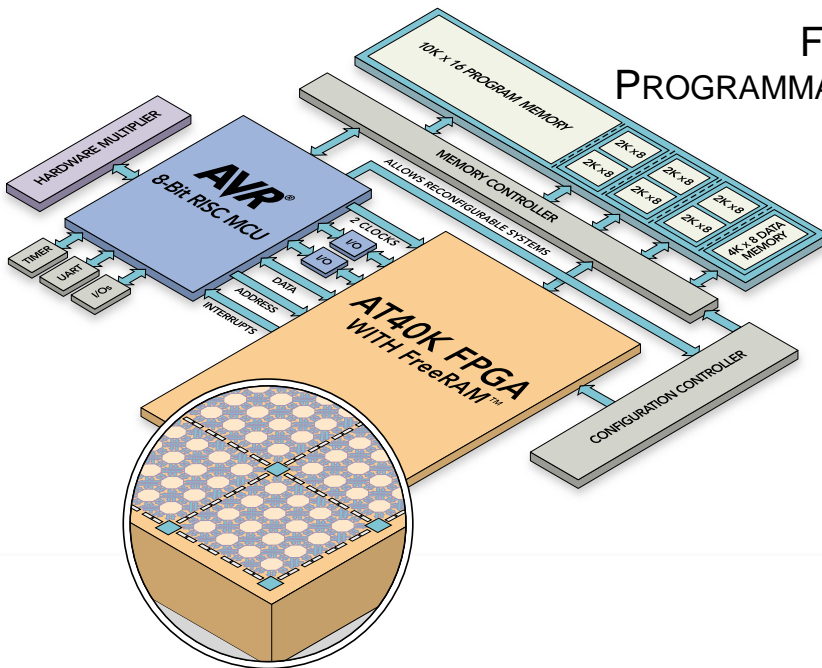


FIELD PROGRAMMABLE

SYSTEM LEVEL INTEGRATED CIRCUIT

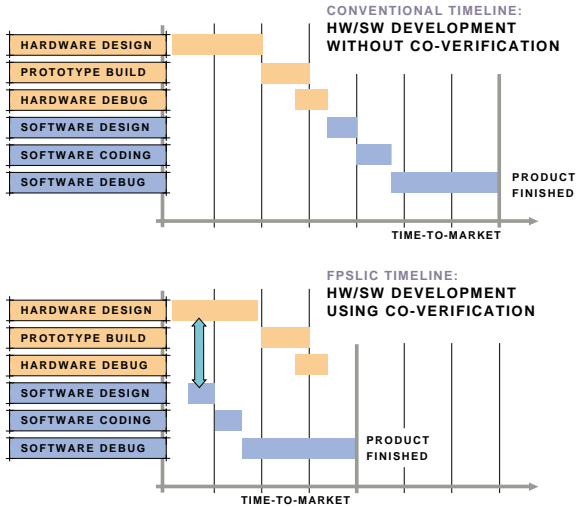


The FP SLIC™ (Field Programmable System Level Integrated Circuit) family of devices incorporates up to 40,000 gates of AT40K FPGA, 36K bytes of SRAM, the 30 MIPS 8-bit AVR® RISC microcontroller core and fixed peripherals on a monolithic device. For the first time all the components of a typical system are available in a high-performance field-programmable device.

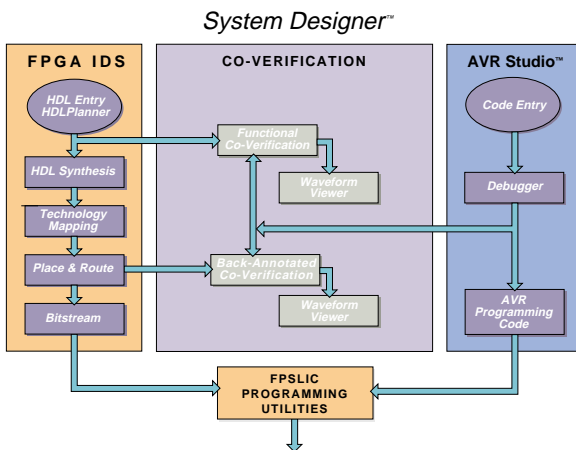
- A monolithic device featuring:
 - 10K, 20K, or 40K gate FPGA
 - 30 MIPS microcontroller performance
 - Ultra-low power consumption
 - In-system reconfigurable
- Completely integrated design tools including:
 - FPGA Integrated Development System
 - AVR Studio
 - Synthesis
 - Simulation
 - Co-verification
- FP SLIC supports:
 - 10K to 40K system-level logic gates
 - Eight global clocks
 - Up to 304 programmable PCI-compliant I/O pins
- Atmel's SRAM-based AT40K FPGA eight-sided logic cell architecture performs complex DSP functions without impacting bus resources
- Discrete FreeRAM™ 10 ns dual-port SRAM blocks are located at the corners of each 4 x 4 cell FPGA sector. Locating these SRAM blocks throughout the array puts memory where it's needed, and supports high-performance FIFO designs
- Atmel's AVR 8-bit RISC microcontroller architecture enables throughput in excess of 30 million instructions per second
- 8-bit hardware multiplication accelerator enables AVR microcontroller to perform complex DSP operations quickly and efficiently
- 32K byte dynamic allocation program memory – a 16K x 16 (32K x 8) block of 15 ns SRAM for program instruction storage. If not all 32K is required, program memory may be partitioned during design development into 4K x 8 blocks to provide additional data memory storage
- 4K byte (4K x 8) data memory (may be increased by adding partitions from program memory)



Atmel has solved the software problems of system integration, debug and testing, by providing a complete system development productivity environment. Co-verification⁽¹⁾ tools allow for concurrent software and hardware development and debug. Design problems are identified earlier in the design process allowing them to be fixed quickly, minimizing their impact on project schedules.



By combining industry-standard development tools and tried and tested design methodology the System Designer™ software is a system architects dream. We have taken mature tools and combined them with standard third-party design entry and verification tools to provide the ideal environment for rapid, bug free development and “what if” analysis. Make trade-offs between software and hardware implementations of an algorithm. Save power by running complex DSP functions in FPGA instead of software. Reconfigure FPGA on-the-fly from the microcontroller to update your latest encryption algorithm. Create your product with the interfaces and peripheral on it needed to make your designs fly.



Note: 1. Co-verification provided by Mentor Graphics.

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