AT40K Series Configuration

Configuration is the process by which a design is loaded into an AT40K series field programmable gate array (FPGA). AT40K series devices are SRAM based and can be configured any number of times. The entire device or select portions can be configured. Sections can be configured while others continue to operate undisturbed. Full configuration takes only milliseconds. Partial configuration takes even less time and is a function of design density.

Configuration data is transferred to the device in one of six modes (Table 1). Three dedicated input pins, M_0, M_1, and M_2, determine the configuration mode. There is one auto-configuring Master mode, four Slave modes, and a Synchronous RAM mode for accessing the SRAM based configuration memory directly from a parallel microprocessor port.

Configuration States

There are four basic configuration states of operation. The first, power-on-reset, occurs when power is first applied to the part. The FPGA initiates a complete clearing of all internal configuration SRAM (configuration clear cycle).

The second, manual reset, occurs when the RESET pin is driven low by the user. Again, the FPGA initiates a configuration clear cycle.

The third is configuration download. In this state the Configuration Mode is active. The FPGA accepts serial or parallel data from an outside source and configures the configuration SRAM appropriately.

The fourth is idle, when there is no configuration activity.

Table 1. AT40K Series Configuration Modes

Mode	Description	M_2	M_1	M_0	CCLK	Data	Notes
0	Master Serial	0	0	0	Output	Serial	Auto Configuration, Serial EEPROM
1	Slave Serial	0	0	1	Input	Serial	Microprocessor or Serial EEPROM
7	Slave Serial	1	1	1	Input	Serial	Microprocessor or Serial EEPROM
2	Slave Parallel	0	1	0	Input	8- or 16-bit Word	Microprocessor or Parallel EEPROM
6	Slave Parallel UP	1	1	0	Input	8- or 16-bit Word	20-bit Address Out, Parallel EPROM
4	Synchronous RAM	1	0	0	Input	8- or 16-bit Word	24-bit Address In, Parallel Port of Microprocessor

AT40K FPGAs

Application Note

Rev. 1009A–01/99

Master Mode

The master mode is auto-configuring; that is, after power-on-reset (POR) and the clearing of configuration memory, it self-initiates configuration. The master mode uses an internal oscillator to provide CCLK for clocking the external EEPROMs (Configurators) which contain the configuration data. CCLK also drives the downstream devices (Slaves) in the configuration cascade chain. Master Serial mode clocks and receives data from a EEPROM Serial Configuration Memory (AT17C65, AT17C128, AT17C256, AT17C512, AT17C010). After auto-configuration is complete, reconfiguration can be initiated manually by the user.

Slave Modes

In slave modes, configuration is always initiated by an external signal. Data is applied to the device on the rising edge of CCLK. In Slave Serial Mode, the device receives serial configuration data. In Slave Parallel Mode, the device receives either 8-bit wide or 16-bit wide parallel data. In Slave Parallel Up Mode, the device receives either 8-bit or 16-bit wide parallel data and generates a 20-bit address up counter for use in addressing memories. CCLK is not generated in slave modes.

Synchronous RAM Mode

In Synchronous RAM Mode, the device receives a 32- or 40-bit wide bitstream composed of a 24-bit address and either a 8-bit wide or 16-bit wide word of data. Address, data, and write enable are applied simultaneously at the rising edge of CCLK. In this mode, designed to interface to a generic IO port of a microprocessor, the FPGA configuration SRAM is seen as a simple memory mapped address space. The user has full read and write access to the entire FPGA configuration SRAM. The overhead normally associated with bitstreams is eliminated, resulting in faster reconfiguration.

Configuration Pins

During configuration, the flow of design data to and from the device is controlled by the dedicated mode pins and a number of dual function pins that double as user I/O under normal programmed operation. The number of dual function pins required for each mode varies (Table 2).

Table 2. Configuration Pins Interface Definition

	State							
Pins	**Reset**	**Download Mode 0**	**Download Mode 1**	**Download Mode 7**	**Download Mode 2**	**Download Mode 6**	**Download Mode 4**	**Idle**
$M_{(2:0)}$	TTL Input	TTL Input	TTL Input	TTL Input	TTL Input	TTL Input	TTL Input	TTL Input
RESET	TTL Input, 50K Pullup	TTL Input, 50K Pullup	TTL Input, 50K Pullup	TTL Input, 50K Pullup	TTL Input, 50K Pullup	TTL Input, 50K Pullup	TTL Input, 50K Pullup	TTL Input, 50K Pullup
INIT	Open Drain Bidirectional, 20K pullup	Open Drain Bidirectional, 20K pullup	Open Drain Bidirectional, 20K pullup	Open Drain Bidirectional, 20K pullup	Open Drain Bidirectional, 20K pullup	Open Drain Bidirectional, 20K pullup	Open Drain Bidirectional, 20K pullup	User I/O
CON	Open Drain Bidirectional, 10K pullup	Open Drain Bidirectional, 10K pullup	Open Drain Bidirectional, 10K pullup	Open Drain Bidirectional, 10K pullup	Open Drain Bidirectional, 10K pullup	Open Drain Bidirectional, 10K pullup	Open Drain Bidirectional, 10K pullup	Open Drain Bidirectional, 10K pullup
CCLK	Schmitt trigger Input, 50K pullup	Output	Schmitt trigger Input, 50K pullup	Schmitt trigger Input, 50K pullup	Schmitt trigger Input, 50K pullup	Schmitt trigger Input, 50K pullup	Schmitt trigger Input, 50K pullup	Schmitt trigger Input, 50K pullup
HDC	Output	Output	Output	Output	Output	Output	User I/O	User I/O
LDC	Output	Output	Output	Output	Output	Output	User I/O	User I/O
D_0	CMOS Input, 20K pullup	Input	Input	Input	Input	Input	Bidirectional	User I/O
$D_{(7:1)}$	CMOS Input, 20K pullup	User I/O	User I/O	User I/O	Input	Input	Bidirectional	User I/O
$D_{(15:8)}$	CMOS Input, 20K pullup	User I/O	User I/O	User I/O	Optional Input	Optional Input	Optional Bidirectional	User I/O
$A_{(19:0)}$	CMOS Input, 20K pullup	User I/O	User I/O	User I/O	User I/O	Output	Input	User I/O

Table 2. Configuration Pins Interface Definition (Continued)

Pins	State							
	Reset	Download Mode 0	Download Mode 1	Download Mode 7	Download Mode 2	Download Mode 6	Download Mode 4	Idle
$A_{(23:20)}$	CMOS Input, 20K pullup	User I/O	User I/O	User I/O	User I/O	User I/O	Input	User I/O
CS0	CMOS Input, 20K pullup	User I/O	Input	User I/O	User I/O	User I/O	Input	User I/O
CS1	CMOS Input, 20K pullup	User I/O	User I/O	User I/O	Input	User I/O	User I/O	User I/O
CSOUT	CMOS Input, 20K pullup	Optional Output	Optional Output	Optional Output	Optional Output	Optional Output	User I/O	User I/O
CHECK	CMOS Input, 20K pullup	Check Input or User I/O	Check Input or User I/O	Check Input or User I/O	Check Input or User I/O	Check Input or User I/O	Check Input or User I/O	User I/O
OTS	CMOS Input, 20K pullup	OTS Input or User I/O	OTS Input or User I/O	OTS Input or User I/O	OTS Input or User I/O	OTS Input or User I/O	OTS Input or User I/O	OTS Input or User I/O

M_0, M_1, M_2

The mode pins are dedicated TTL threshold inputs that determine the configuration mode to be used. Table 1 lists the states for each configuration mode. The mode pins should not be changed during power-on-reset, manual reset, or configuration download. The user may change the mode pins during configuration idle. These pins have no pullup resistors to VDD, so they need to be driven by the user or tied off.

CCLK

CCLK is the configuration clock pin. It is an input or output depending on the mode of operation. During power-on-reset or manual reset, it is a tristated output. During configuration download and in Mode 0, it is an output with a typical frequency of 1 MHz. During configuration download and in all other modes, it is a schmitt trigger input with approximately 1 volt of hysteresis for noise immunity. It is an input during configuration idle, but is ignored. It is pulled to VDD with a nominal 50K internal resistor.

RESET

RESET is the FPGA configuration manual reset pin. It is available during all configuration states. It initiates a configuration clear cycle and, if operating in Mode 0, an auto-configuration. It is a dedicated schmitt trigger input with approximately 1 volt of hysteresis for noise immunity. It is pulled to VDD with a nominal 50K internal resistor.

INIT

INIT is a multi-function pin. During power-on-reset and manual reset, the pin functions as an open drain bidirectional I/O which releases high when the configuration clear cycle is complete, but can be held low to hold the configuration in a reset state. Once released, the FPGA will proceed to either configuration download or idle, as appropriate. During configuration download, the INIT pin is again an open drain bidirectional pin which signals if an error is encountered during the download of a configuration bitstream. In addition, during the Check Function, the INIT pin drives low for any configuration SRAM mismatch (see the description of the Check Function on page 11 for more details). While in open drain mode, the pin is pulled to VDD with a nominal 20K internal resistor. When not configuring, the INIT pin becomes a fully functional user I/O.

CON

CON is the FPGA configuration start and status pin. It is a dedicated open drain bidirectional pin. During power-on-reset or manual reset, CON is driven low by the FPGA. In Modes 2, 6, or 7, when the FPGA has finished the configuration clear cycle, CON is released to indicate the device is ready for the user to initiate configuration download. The user may then drive CON low to initiate a configuration download. After three clock cycles, CON is then driven low by the FPGA until it finishes the download, and it is then released. In Mode 0, CON is not released by the FPGA at the end of power-on-reset or manual reset. Instead, CON is controlled by the FPGA until the end of the auto-configuration process. CON is released at the end of configuration download in Mode 0, and the user may then initiate a manual configuration download by driving CON low. While in open drain mode, the pin is pulled to VDD with a nominal 10K internal resistor.

HDC

HDC is the FPGA "High During Configuration" pin. It is an output, driven high by the FPGA during power-on-reset, manual reset, and configuration download. During configuration idle, the pin is a fully functional user I/O.

Note: All user I/O default to inputs with pullups "on". The HDC pin transitions from driving a strong "1" to a pullup "1" after reset. The HDC pin will transition from driving a strong "1" to the user programmed state at the end of configuration download. If not programmed, the default state is input with pullup.

LDC

LDC is the FPGA "Low During Configuration" pin. It is an output, driven low by the FPGA during power-on-reset, manual reset, and configuration download. During configuration idle, the pin is a fully functional user I/O.

Note: All user I/O pullups and pulldowns are programmed by the user. The LDC pin transitions from driving a strong "0" to a weak "1" after reset. The LDC pin will transition from driving a strong "0" to the user programmed state at the end of configuration download. If not programmed, the default state is input with pullup.

D_0

D_0 is the lsb of the FPGA configuration data bus used to download configuration data to the device. During power-on-reset or manual reset, D_0 is controlled by the configuration SRAM. The D_0 pin will transition from the user programmed state to a CMOS input with a nominal 20K internal pullup resistor as the SRAM at that location is cleared by the configuration clear cycle. D_0 becomes an input during configuration download.

D_1:D_7

D_1:D_7 are the upper 7 bits of the 8-bit parallel data bus used to download configuration data to the device. During power-on-reset or manual reset, D_1:D_7 are controlled by the configuration SRAM. The D_1:D_7 pins will transition from the user programmed state to CMOS inputs with nominal 20K internal pullup resistors as the SRAM at those locations is cleared by the configuration clear cycle. When in Modes 2 or 6, D_1:D_7 become inputs during configuration download. D_1:D_7 are not used in the serial Modes 0, 1 and 7.

D_8:D_{15}

D_8:D_{15} are the upper 8 bits of the 16-bit parallel wide data bus used to download configuration data to the device. During power-on-reset or manual reset, D_8:D_{15} are controlled by the configuration SRAM. The D_8:D_{15} pins will transition from the user programmed state to CMOS inputs with nominal 20K internal pullup resistors as the SRAM at those locations is cleared by the configuration clear cycle. When in Modes 2 or 6, D_8:D_{15} become optional inputs during configuration download. They become available as soon as the appropriate bit in the configuration control register is set. D_8:D_{15} are not used in the serial Modes 0, 1 and 7.

A_0:A_{19}

A_0:A_{19} are used to control external addressing of memories during downloads. During power-on-reset or manual reset, A_0:A_{19} are controlled by the configuration SRAM. The A_0:A_{19} pins will transition from the user programmed state to CMOS inputs with nominal 20K internal pullup resistors as the SRAM at those locations is cleared by the configuration clear cycle. When in Mode 6, A_0:A_{19} become outputs during configuration download. A_0:A_{19} are used only in Mode 6.

Note: Pin A_2 is also pin CS_1, which is available only for Mode 2. See the description for CS_1 on page 5 for more details.

CS_0

CS_0 is an FPGA configuration chip select. It is active low. During power-on-reset or manual reset, CS_0 is controlled by the configuration SRAM. The CS_0 pin will transition from the user programmed state to a CMOS input with a nominal 20K internal pullup resistor as the SRAM at that location is cleared by the configuration clear cycle. In Mode 1, it is used as a chip select to enable configuration to begin. It is most often used as the chip select of the downstream device in a cascade chain, and is usually driven by CSOUT of the upstream device. Releasing CS_0 during configuration causes the Mode 1 FPGA to abort the download and release CON. CS_0 is used only in Mode 1.

CS_1

CS_1 is an FPGA configuration chip select. It is active low. During power-on-reset or manual reset, CS_1 is controlled by the configuration SRAM. The CS_1 pin will transition from the user programmed state to a CMOS input with a nominal 20K internal pullup resistor as the SRAM at that location is cleared by the configuration clear cycle. In Mode 2, it is used as a chip select to enable configuration to begin. It is most often used as the chip select of the downstream device in a cascade chain, and is usually driven by CSOUT of the upstream device. Releasing CS_1 during configuration causes the Mode 2 FPGA to abort the download and release CON. CS_1 is used only in Mode 2.

Note: Pin CS_1 is also pin A2, which is active only for Mode 6. See the description for A_0:A_{19}, on page 4 for more details.

CSOUT

CSOUT is the configuration pin used to enable the downstream device in a cascade chain. During power-on-reset or manual reset, CSOUT is controlled by the configuration SRAM. The CSOUT pin will transition from the user programmed state to a CMOS input with a nominal 20K internal pullup resistor as the SRAM at that location is cleared by the configuration clear cycle. During configuration download, CSOUT becomes an optional output. It is enabled by default after reset, and may be enabled or disabled via the configuration control register. If the user has disabled the cascade function, the pin remains a user I/O. If the cascade function is enabled, the CSOUT pin is driven high at the start of configuration download. At the end of the device's portion of the cascade bitstream, the CSOUT pin is driven low (and into the CS_0 or CS_1 of the downstream device) to enable the downstream device. CSOUT is released by the device at the end of the cascade bitstream and becomes a fully functional user I/O.

CHECK

CHECK is a configuration control pin used to control the Check Function. The Check Function takes a bitstream and compares it to the contents of a previously loaded bitstream and notifies the user of any differences. Any differences causes the INIT pin to go low. During power-on-reset or manual reset, CHECK is controlled by the configuration SRAM. The CHECK pin will transition from the user programmed state to a CMOS input with a nominal 20K internal pullup resistor as the SRAM at that location is cleared by the configuration clear cycle. During configuration download, CHECK becomes an optional input. It is enabled by default after reset, and may be enabled or disabled via the configuration control register. If the user has disabled the Check Function, the pin remains a user I/O.

OTS

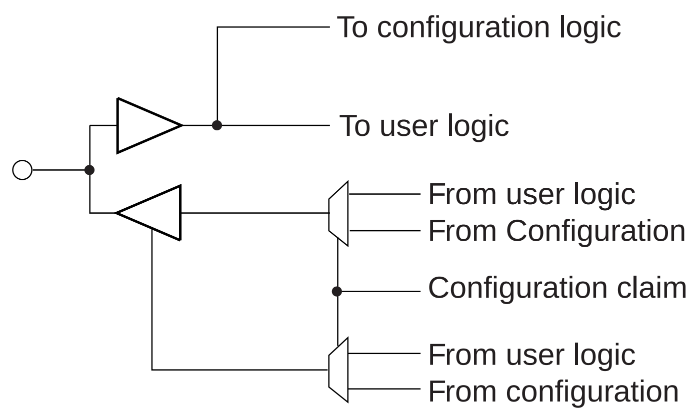
OTS is an input pin used to immediately tristate all user I/O. It is enabled by a bit in the configuration control register. Once activated, it is always an input. The OTS tristate control of Dual Use pins is superseded by the configuration logic's claim on those pins. If the user has disabled the OTS function, the pin remains as User I/O.

Dual Use I/O

Any pin which functions as user I/O and configuration I/O is a Dual Use I/O pin. INIT, HDC, LDC, D_0:D_{15}, A_0:A_{19}, CS_0, CS_1, CSOUT, CHECK, and OTS are all Dual Use I/O pins. It must be noted that while the configuration logic controls Dual Use I/O pins during a particular mode of operation, the configuration logic does not control the pullup, pulldown, CMOS/TTL threshold select, or Schmitt trigger selects. The user must be cautioned to avoid possible system problems with the use of Dual Use I/O pins. For example, turning off the internal pullup resistor for the open drain INIT pin would not apply the weak high required of an open drain driver. Conversely, disabling the pullup and enabling the pulldown of the HDC pin might be a good idea, since the user may then actually see the pin go low at the end of configuration.

Dual Use pins share input buffers. It should be noted that even when the configuration has claimed a pin for its own purposes, the user input buffer is still fully functional. This implies that any user logic tied to the input buffers of the pins in question will remain operational. (See Figure 1).

Figure 1. Dual Use IO



Configuration States

When power is first applied to an AT40K series FPGA, an internal power-on-reset circuit senses VDD and activates at approximately 2.1 volts. The FPGA then enters the power-on-reset state. During this state, INIT is driven low, CON is driven low, LDC is driven low, HDC is driven high, and all user I/O are tristated. I/O thresholds, pullups and pulldowns are at an indeterminate state. The FPGA configuration clear cycle begins and the configuration SRAM is reset. The configuration clear cycle is repeated a nominal 150 ms to allow VDD to rise to the minimum operational level for the device (3.0 volts).

This additional delay is only applied at power-on-reset, and is not needed for manual reset.

Once the configuration clear cycle is complete, RESET is sampled. If high, INIT is released. This open drain pin is sampled to make sure all other devices (if any) in a cascade chain are also done with the configuration clear cycle. Once INIT goes high the mode pins are sampled.

If Mode 0 is detected, the part proceeds to the configuration download state. CON is held low by the FPGA, HDC remains high, LDC remains low, and CCLK is now driven by the FPGA at a nominal frequency of approximately 1 MHz. The appropriate configuration interface pins for Mode 0 become active.

If a slave mode is detected (i.e., Modes 1, 2, 6, or 7), then CON is released and pulled high with the internal pullup resistor. Once CON goes high, the part proceeds to the idle state and LDC and HDC are released. The internal oscillator stops running. The part is now available for configuration download.

When RESET is lowered, the manual reset state is entered. An internal oscillator begins running, INIT is driven low, CON is driven low, LDC is driven low, and HDC is driven high. During this state, the FPGA configuration clear cycle begins and the configuration SRAM is reset. Once this cycle is complete, RESET is sampled and the reset state machine proceeds as above. The configuration reset state diagram is shown in Figure 2.

Table 3. Configuration Clear Cycle Times

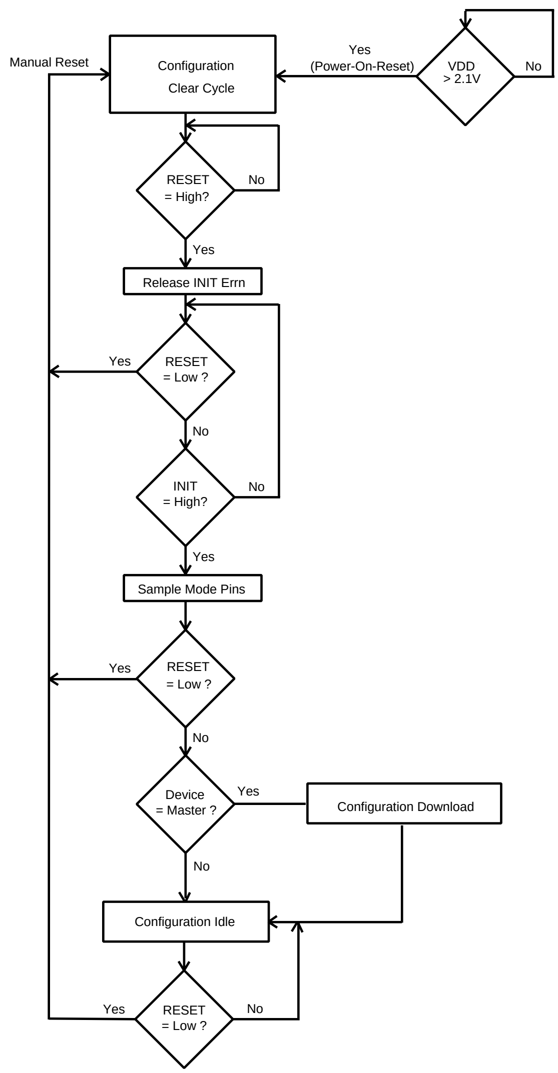
Device	Array Size	Clear Cycle Time			Units
		Min	Typ	Max	
AT40K05	16 x 16	137	228	365	µs
AT40K10	24 x 24	197	328	525	µs
AT40K20	32 x 32	257	428	685	µs
AT40K30	40 x 40	317	528	845	µs
AT40K40	48 x 48	377	628	1005	µs

After a configuration clear cycle, the user logic of the FPGA is set to a benign state. The following chart shows the various types of user circuitry and their default states.

Core	inputs tied off local drivers off DFF set
Repeater	all drivers off passgates off
I/O	output drivers off CMOS threshold pullup enabled pulldown disabled
Clocks	tied high
Resets	tied low (active)
RAM	disabled contents cleared

There is no activity in either the user logic or the configuration logic and the device is in a low power state.

Figure 2. Configuration Reset State Diagram



The AT40K FPGA allows complete reconfigurability down to the byte level. The CacheLogic® architecture lets users reconfigure part of the FPGA while the rest of the FPGA continues to operate unaffected.

Control of the FPGA system level interface is possible on an AT40K series FPGA. User I/O, internal Global Set/Reset, and Global and Fast Clocks can be enabled or disabled during configuration downloads by setting bits in the control register.

User I/O become active as soon as the relevant I/O configuration SRAM is loaded. To aid system level integration, a bit in the control register (CR_{31}) may be set which commands all I/O pins not part of the configuration interface to go tristated. This bit is set at the start of configuration so the very first download can be affected.

Another bit in the control register (CR_{30}) may be set to enable (drive low) the global reset net during configuration download.

Another set of bits in the control register (CR_{27}:CR_{16}) may be set to disable (drive high) each of the global and fast clock input buffers which drive the global clock nets. The user I/O portion of these buffers is not affected.

Holding off Auto-Configuration

There are two methods by which the user may delay a master Mode 0 auto-configuration. The first is to drive RESET low during power-on-reset or manual reset and hold the signal low until the user is ready to proceed with auto-configuration. The second is to drive INIT low with an open drain driver during power-on-reset or manual reset, and release when the user is ready to proceed with auto-configuration. Both are valid in a AT40K series device. Assuming the device has completed its configuration clear cycle and that INIT and RESET are inactive (high), a Mode 0 FPGA starts CCLK and configuration download.

Configuration Control Register

The AT40K series devices have a 32-bit control register that is written at the beginning of a configuration download. These bits control various configuration sequence parameters. All bits are set to 0 during a configuration clear cycle. In parallel modes, byte 0 is loaded first. In serial modes, bit-31 is loaded first. The control register settings are made in the FPGA Designer IDS Software Options section.

Table 4. Control Register

Byte 0	CR_{31}	CR_{30}	CR_{29}	CR_{28}	CR_{27}	CR_{26}	CR_{25}	CR_{24}
Byte 1	CR_{23}	CR_{22}	CR_{21}	CR_{20}	CR_{19}	CR_{18}	CR_{17}	CR_{16}
Byte 2	CR_{15}	CR_{14}	CR_{13}	CR_{12}	CR_{11}	CR_{10}	CR_9	CR_8
Byte 3	CR_7	CR_6	CR_5	CR_4	CR_3	CR	CR_1	CR_0

CR_0: 0 = Reset Address Counter
1 = Retain Address Counter

CR_0 controls the value of the Mode 6 device's memory address counter after each configuration sequence. The default resets the address up-counter to 000000 after each configuration download is completed. When this bit is set, the memory address counter retains its last value. This allows multiple designs to be stored sequentially in an external memory device for use in reconfigurable systems.

CR_1: Not used (ignored)

CR_2: 0 = Enable cascading
1 = Disable cascading

CR_2 controls the operation of the dual function I/O CSOUT. When CR_2 is set, the CSOUT pin is not used by the configuration during downloads.

CR_3: 0 = Check function enabled
1 = Check function disabled

CR_3 controls the operation of the CHECK pin and enables the Check Function. When CR_3 is set, the CHECK pin is not used by the configuration during downloads.

CR_4: 0 = Memory Lockout disabled
1 = Memory Lockout enabled

CR_4 is the Security Flag and controls the writing and checking of configuration memory during any subsequent configuration download. When CR_4 is set, any subsequent configuration download initiated by the user, whether a normal download or a CHECK function download, causes the INIT pin to immediately activate. CON is released, and no further configuration activity takes place. The download sequence during which CR_4 is set is NOT affected. The Control Register write is also prohibited, so bit CR_4 may only be cleared by a power-on-reset or manual reset.

CR_5: Not used (ignored)

CR_6: 0 = OTS disabled
1 = OTS enabled

Setting CR_6 makes the OTS pin an input which controls the global tristate control for all user I/O.

CR_7: 0 = 8-bit data access
1 = 16-bit (Wide) data access

CR_7 is the Wide data control bit. Setting this bit immediately enables bits D_8:D_{15} of the configuration interface as inputs for all parallel modes (2 and 6). All writes and checks of configuration memory are subsequently performed by 16 bits. Cr_7 is ignored in serial modes (0, 1 and 7).

CR_8: Not used (ignored)

CR_9: Not used (ignored)

CR_{10}: Not used (ignored)

CR_{11}: Not used (ignored)

CR_{12}: Not used (ignored)

CR_{13}: 0 = CCLK normal operation
1 = CCLK continues after configuration

Setting bit CR_{13} allows the CCLK pin to continue to run after configuration download is completed. This bit is valid for master mode.

CR_{14}:CR_{15}: 00 = 1 MHz
01 = 2 MHz
10 = 4 MHz
11 = 8 MHz

Bits CR_{14} and CR_{15} speed up the internal oscillator and allow the master mode to drive CCLK at 1, 2, 4 or 8 MHz. Setting these bits immediately enables the higher CCLK frequency.

CR_{16}:CR_{23}: 0 = Gclk0:7 always enabled
1 = Gclk0:7 disabled during configuration download.

Setting CR_{16}:C_{23} allows the user to disable the input buffers driving the global clocks. The clock buffers are enabled and disabled synchronously with the rising edge of the respective Gclk signal, and stop in a high ("1") state. Setting one of these bits disables the appropriate Gclk input buffer only and has no effect on the connection from the input buffer to the FPGA array.

CR_{24}:CR_{27}: 0 = Fclk0:3 always enabled
1 = Fclk0:3 disabled during configuration download.

Setting CR_{24}:C_{27} allows the user to disable the input buffers driving the fast clocks. The clock buffers are enabled and disabled synchronously with the rising edge of the respective Fclk signal, and stop in a high ("1") state. Setting one of these bits disables the appropriate Fclk input buffer only and has no effect on the connection from the input buffer to the FPGA array.

CR_{28}: Reserved (must be "0")

CR_{29}: Not used (ignored)

CR_{30}: 0 = Global set/reset normal

1 = Global set/reset active (low) during configuration

CR_{30} allows the Global set/reset hold the core DFFs in set/reset during any configuration download. The Global set/reset net is released at the end of configuration download on the rising edge of CON.

CR_{31}: 0 = Disable I/O tristate

1 = I/O tristate during configuration

CR_{31} forces all user defined I/O pins to go tristate during configuration download. Tristate is released at the end of configuration download on the rising edge of CON.

Configuration Downloads

The initiation of the writing, reading, or checking design specific data into the FPGA configuration SRAM is called configuration download. Configuration downloads are executed by a synchronous state machine that controls the flow of data into the FPGA (Figure 3). The state machine is clocked by CCLK. On the rising edge of each CCLK a bit or byte of the configuration data bitstream is clocked into the device. Figure 5 displays a sample 8-bit wide bitstream for an AT40K series device.

Figure 3. Configuration Download State Machine

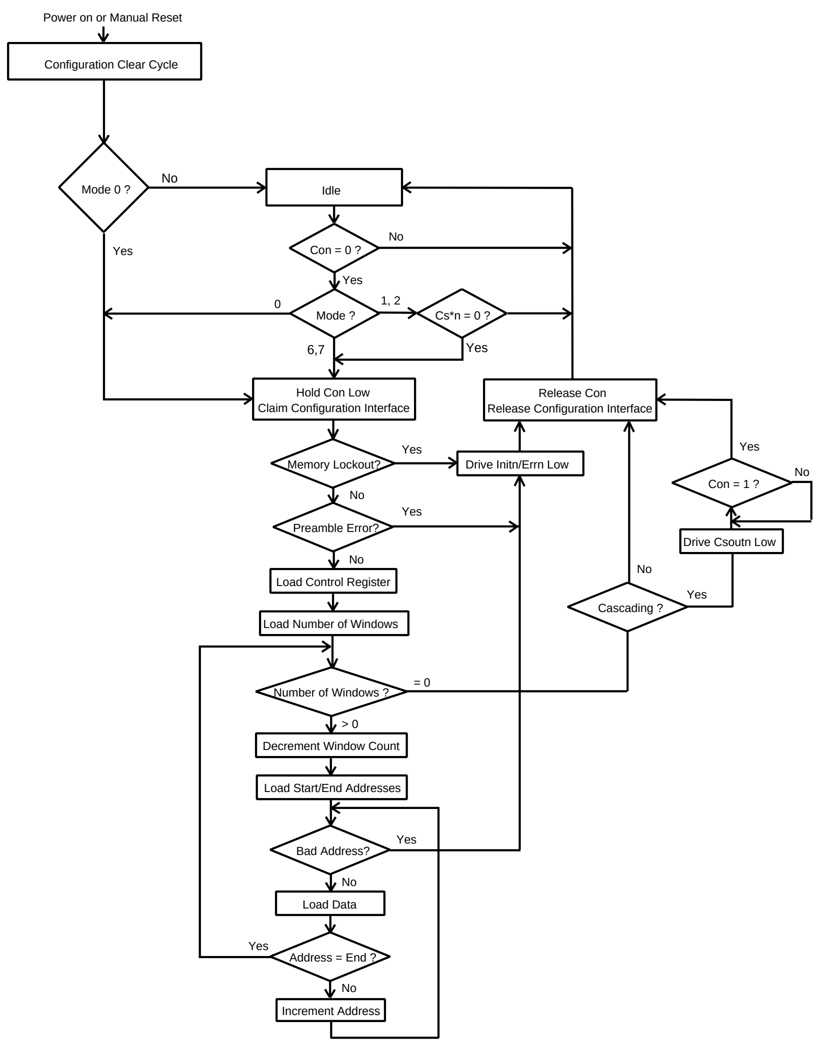


Table 5. Sample 8-bit wide stream

msb<>lsb	
00000000	null
10110111	preamble
00000000	control register byte 0
00000000	control register byte 1
00000000	control register byte 2
00000000	control register byte 3
00000000	number of windows, msb
00000001	number of windows, lsb
00000000	start address 0
00000000	start address 1
00000000	start address 2
00000000	end address 0
00000000	end address 1
00000011	end address 2
11110000	data, byte 0
11100001	data, byte 1
11010010	data, byte 2
11000011	data, byte 3
11100111	postamble

From the power-on-reset, manual reset, or the configuration idle state, when CON and the appropriate chip select (CS_0 or CS_1) is activated, the device begins clocking data. For AT40K series devices, the timing relationships are fixed, and no additional data is allowed at the front of the bitstreams. Serial data is read in most-significant-bit first.

The null byte is read in, followed by the preamble. If the expected preamble value is not seen as the second byte of data, an error is reported by driving INIT low and terminating the configuration download.

After the preamble check, the state machine loads the configuration control register, which controls various features of the configuration process.

Small areas of the AT40K arrays can be programmed independently of each other. Each of these areas is known as a window. After the control register, the device loads the number of configuration windows. A single bitstream can have up to 64K windows. The minimum data block size for a window is 1 word.

Next, the start and end addresses of the first window are loaded. An invalid start address will cause an error; the INIT pin is driven low, and the configuration download is terminated.

Next, data is loaded into the configuration SRAM (unless the CHECK function is activated).

Next, if more than one window is to be downloaded, start and end addresses are loaded, followed by another data block. This process is repeated until all windows are downloaded.

Finally, the postamble byte is downloaded. If the expected postamble value is not seen as the last byte of data, an error is reported by driving INIT low and terminating the configuration download.

Wide Data Configuration Downloads

For parallel Modes 2 and 6, there is available an option to increase the bandwidth of the data block portion of the download to 16-bits per clock cycle, reducing download time. Table 6 shows a sample 16-bit version of the same 8-bit bitstream shown in Table 5.

Table 6. Sample 16-bit wide bitstream

msb lsb	
xxxxxxxx00000000	null
xxxxxxxx10110111	preamble
xxxxxxxx00000000	control register byte 0
xxxxxxxx00000000	control register byte 1
xxxxxxxx00000000	control register byte 2
xxxxxxxx10000000	control register byte 3
xxxxxxxx00000000	number of windows, msb
xxxxxxxx00000001	number of windows, lsb
xxxxxxxx00000000	start address 0
xxxxxxxx00000000	start address 1
xxxxxxxx00000000	start address 2
xxxxxxxx00000000	end address 0
xxxxxxxx00000000	end address 1
xxxxxxxx00000011	end address 2
1110000111110000	data: byte1, byte0
1100001111010010	data: byte1, byte0
xxxxxxxx11100111	postamble

Note: x is a don't care

As can be seen from the figure only the data block portion of the download has increased bandwidth. The upper 8-bits of all other non-data words can be treated as don't cares. To turn on the wide interface, a bit is set in the control register. Once set, the configuration claims the upper 8 Dual Use I/O data pins (D_8:D_{15}). This implies that at the start of a parallel download in which the user wants wide data bandwidth and D_8:D_{15} as user output ports, the configuration interface pins D_8:D_{15} will not be tristated until the appropriate byte of the control register is written. At the start of any subsequent reconfigurations, pins D_8:D_{15} will be claimed immediately upon CON going low. Atmel recommends not moving between 8- and 16-bit data bandwidths.

Full vs. Partial Bitstreams

In programming an AT40K series FPGA, the user will normally load the entire configuration SRAM memory map from start to finish. This requires a full bitstream. Bitstream sizes are shown in Table 7.

Table 7. AT40K Series Bitstream sizes

Device	Array Size	Bytes	Bits
AT40K05	16 x 16	5263	42104
AT40K10	24 x 24	11175	89400
AT40K20	32 x 32	19279	154232
AT40K30	40 x 40	29575	236600
AT40K40	48 x 48	42063	336504

It is possible, by using the windowing mechanism, to download the SRAM memory map in smaller segments. By this means, the user may load portions of the array before others, eliminate the loading of unused portions of the array, and overwrite previously written portions of configuration SRAM with new design information.

AT40K software tools (Atmel's FPGA Integrated Development System) supports bitstream compression. Please refer to the IDS Software User Guide for more information.

Check Function

The AT40K family supports a Check Function on configuration SRAM data (a write verify). This is accomplished by normally initiating a configuration download while driving CHECK low. Instead of writing the contents of the bitstream to memory, the contents of memory are instead read and compared to the bitstream on a byte-by-byte basis in the configuration logic. Any differences are reported by driving the INIT pin low. The INIT pin will lower two clocks after the miscompare. The Check Function is available after power-on-reset and manual reset, and can be performed on an "empty" FPGA prior to the first programming of the device. Windowed or non-windowed bitstreams may be checked. Although the check function does not write the FPGA SRAM contents, the configuration control register is written. The configuration control register is not checked. Start and End addresses are examined for integrity, as they are in every download, but only the data at those addresses are "checked". The contents of the Checksum registers cannot be verified with the Check Function.

The maximum CCLK frequency when performing a Check Function is much lower than that of a normal download. Exact timing specifications are listed under the mode descriptions later in this document.

The bitstream will not be terminated on a Check Function error.

Checksum Function

The AT40K family supports a Checksum Function. During a configuration download, an accumulated checksum is calculated after each word (8- or-16 bits) of the bitstream is downloaded to the FPGA. During the bitstream download, the user may write to a series of registers in a special window known as the Checksum Page.

Table 8. Checksum Page

byte 0	Evaluate Checksum, bits 7:0
byte 1	Evaluate Checksum, bits 15:8
byte 2	Seed, bits 7:0
byte 3	Seed, bits 15:8

After power-on-reset, the checksum and seed are cleared to zero. Just prior to the start of a configuration download, the seed value is loaded into the checksum. Whenever the Evaluate Checksum register(s) are written, a new Checksum is calculated. If the new value does not equal "FF" (or "FFFF" for 16-bit operation), The INIT pin is driven low to indicate an error has occurred. Whenever the Seed is written, the Checksum accumulator is also written with the new Seed value.

The bitstream will not be terminated on a Checksum Function error.

Bitstream Errors

The INIT pin is driven low by the FPGA for a number of reasons. In all cases, the INIT pin will be driven low two clocks after the byte which caused the error. Some errors will cause a bitstream to be terminated. Some will not. If a bitstream is terminated, all configuration pins are released by the configuration logic, and the configuration state returns to Idle.

A bad preamble causes the INIT pin to be driven low, and causes the bitstream to be terminated.

A bad window start address or end address causes the INIT pin to be driven low two clocks after the third byte of the end address is seen by the device. The bitstream is terminated.

If the number of windows has been decremented to zero and the expected postamble is not seen by the device, the INIT pin is driven low two clocks after the bad byte is seen by the FPGA. The bitstream is terminated.

During a Check Function, a mismatched write-verify error results in the INIT pin being driven low two clocks after the byte. The INIT pin will remain low until the end of the bitstream. The bitstream will NOT terminate.

If the Security Flag bit was set in the previous bitstream, the FPGA will drive the INIT pin low two clocks after CON was driven low by the user. The bitstream will immediately terminate.

If a checksum error is detected during a bitstream download, the INIT pin is driven low two clocks after the write to the Checksum Page. The INIT pin will remain low until the end of the bitstream. The bitstream will not terminate.

Synchronous RAM Configuration Downloads (Mode 4)

The AT40K family supports the writing and reading of design specific data to or from the FPGA configuration SRAM by means of a simple single port synchronous SRAM type interface. This interface, requires no configuration state machine during the download process. The process starts when CON and CS0 are both lowered. The configuration interface is claimed, and consists of a clock (CCLK), 24-bits of address (A_0:A_{23}), 8-bits of parallel data (D_0:D_7), a Write/Read bar signal (CHECK), and an error flag (INIT). If the wide data select bit is set in the control register, another 8 bits of parallel data pins (D_8:D_{15}) are claimed by the configuration logic. The entire configuration SRAM memory map is available for read/write access by the user. During write cycles, data, address, and W/R signals are presented simultaneously to the device, and the configuration SRAM write occurs on the first falling edge of CCLK after the first rising edge of CCLK. During read cycles, address and W/R signals are presented simultaneously to the device, and valid data is available on the second rising edge of CCLK.

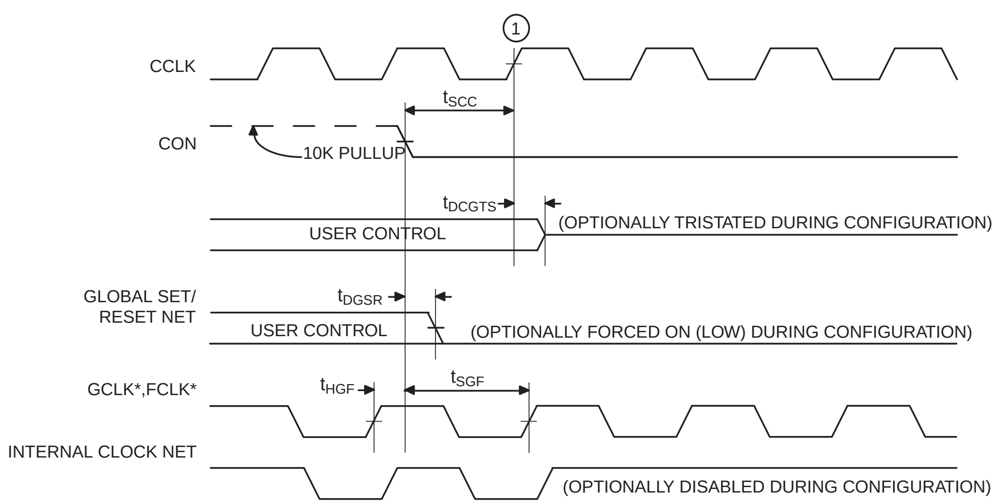
To protect users, detailed bitstream information and detailed use of this mode are not published in this document. For further information on using AT40K devices in dynamically reconfigurable systems using Mode 4, please contact your local Atmel sales office.

Configuration and System Level Integration

To aid in system level integration, AT40K series devices have available a number of bits in the control register which cause the I/O pins to tristate, the Global Set/Reset network to activate (low), and the Global and Fast clock input buffers to be disabled (high).

At the start of configuration, these functions go through a fixed timing sequence whereby they are enabled (if selected by the control register). When CON is driven low by the user, HDC, LDC, INIT and any Dual Use I/O pins needed for the appropriate FPGA mode are claimed immediately by the configuration logic. All I/O not needed by the configuration logic is tristated on the falling edge of CON. The Global Set/Reset net is forced low on the falling edge of CON. The Global and Fast clock nets are disabled (driven high) on the first rising edge of the appropriate Gclk or Fclk signal after the falling edge of CON. Figure 4 shows the timing relationships of these functions at the start of configuration.

Figure 4. System Level Integration: Start of Configuration

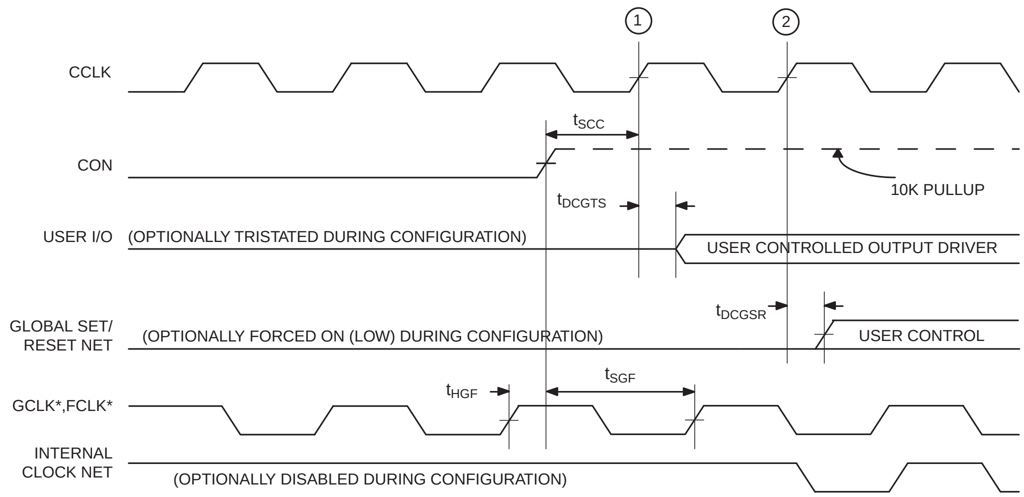


Notes: 1. The appropriate global and fast clock nets are disabled on the first rising edge of the associated global or fast clock input signal after CON is driven low. The nets are forced high for glitchless suppression of activity.

2. User I/O are tristated on the first rising edge of CCLK after CON has been driven low.

At the end of configuration, these functions go through a fixed timing sequence whereby they are disabled. When CON is released and pulled high by the FPGA, HDC, LDC, INIT and any Dual Use I/O pins needed for the appropriate FPGA mode are released immediately by the configuration logic. All other I/O become active (as programmed by the user) on the rising edge of CON. The Global Set/Reset net is released on the second rising edge of CCLK after the rising edge of CON. The Global and Fast clock nets are released on the first rising edge of the appropriate Gclk or Fclk signal after the second rising edge of CCLK after the rising edge of CON. Figure 5 shows the timing relationships of these functions at the end of configuration.

Figure 5. System Level Integration: End of Configuration



Notes:
1. The appropriate global and fast clock nets are enabled on the first rising edge of the associated global or fast cock input signal after CON is released high. The nets are released high for glitchless operation.
2. User I/O output drivers are enabled on the first rising edge of CCLK after CON has been released high.
3. The Global Set/Reset net is no longer forced on (low) on the second rising edge of CCLK after Con has been released high.

Table 9. System Level Integration Timing Parameters @ 5V ± 10% Industrial/Commercial (Not Tested)

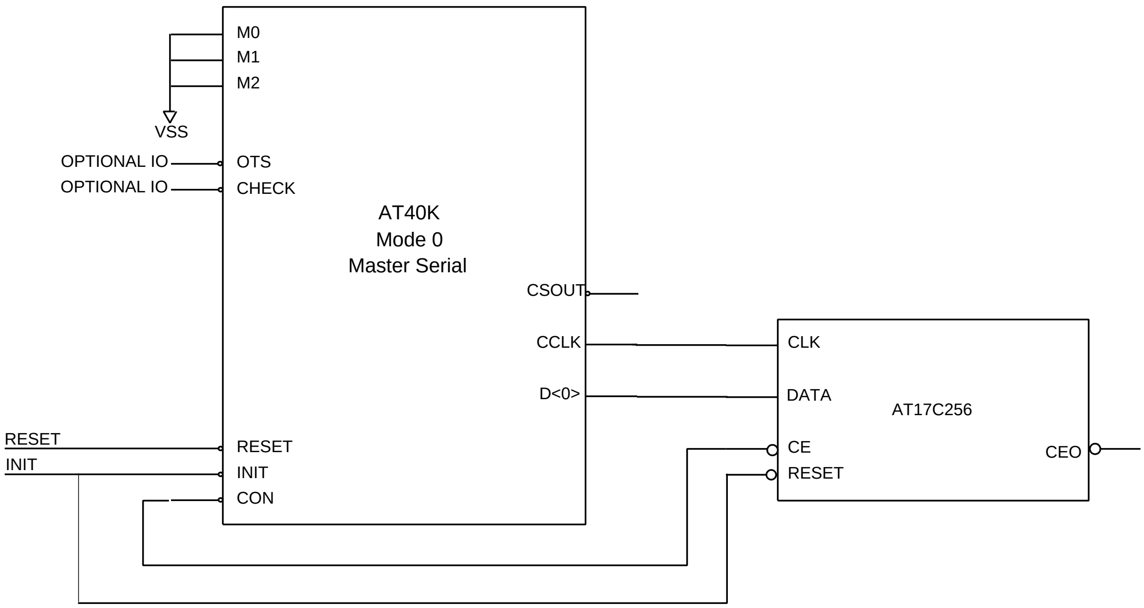
Parameter	Description	Min	Typ	Max	Units
t_{SCC}	Setup time for CON and CS* with respect to CCLK to initiate the start or end of configuration System Startup	6	10	16	ns
t_{DGSR}	Delay from falling edge of CON to a forced low on the Internal Global Set/Rest net	10	16	26	ns
t_{DCGSR}	Delay from rising edge of CCLK to the release of the Internal Global Set/Reset net to full user control	10	16	26	ns
t_{DCGTS}	Delay from rising edge of CCLK to the activation or deactivation of output drivers on User I/O	10	16	26	ns
t_{HGF}	Hold time for the rising edge of Gclk of Fclk with respect to the rising or falling edge of CON for activation or deactivation of one of the Global or Fast Clock nets	0	0	0	ns
t_{SGF}	Setup time for the rising edge of Gclk or Fclk with respect to the rising or falling edge of CON for activation or deactivation of one of the disabled Global or Fast Clock nets. Varies depending on the Gclk or Fclk chosen.	3		24	ns

During a normal download, the I/O, clock tree, and global set/reset nets are loaded near the very end of configuration. The configuration control register is loaded at the beginning of the bitstream, so the system integration bits for I/O tristate, global and fast clocks, and global set/reset nets can be set while those portions of the FPGA are still inactive. This implies that no system integration problems will occur on the first download after power-on-reset or manual reset.

Mode 0: Master Serial

Configuration Data Source:	Serial EEPROM
Dedicated Configuration Pins:	RESET, CON, M_0, M_1, M_2, CCLK
Dual Use I/O:	D_0, INIT, LDC, HDC
Optional Dual Use I/O:	CSOUT, CHECK.OTS

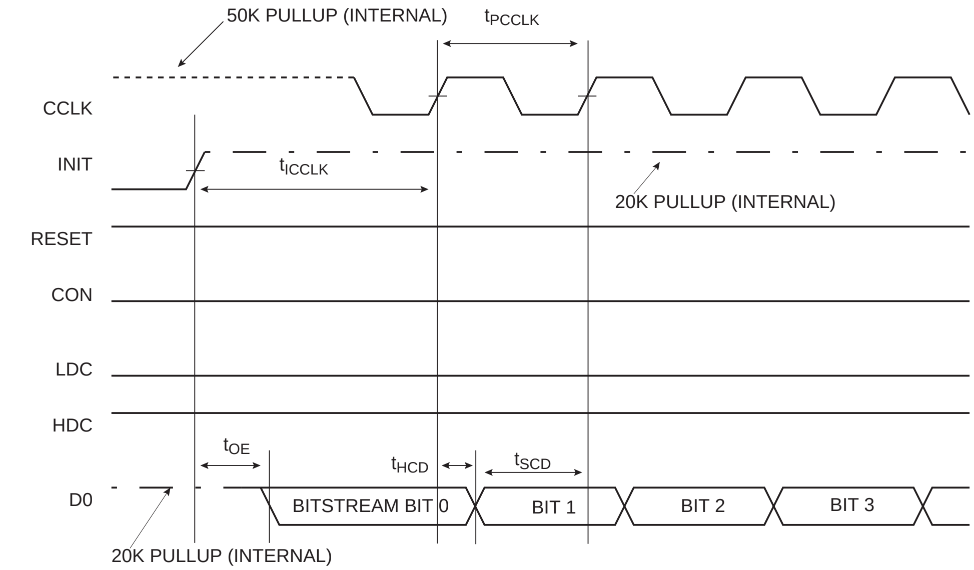
Figure 6. Standalone 0 Configurator System Application



In Mode 0, CCLK is driven by the Master Serial AT40K FPGA into an Atmel Configurator that drives data out its Data pin and into the D0 pin of the FPGA. Each CCLK increments the Configurator internal address counter, and serial data is presented to the FPGA. Once the bitstream is completed, CON is released by the FPGA, indicating the device is completely ready for user operation. Configuration time depends on the frequency of the internal clock driving CCLK (approximately 1 microsecond), and on the structure of the bitstream. A full bitstream for the AT40K20 takes about 153 milliseconds to download (one microsecond per bit of configuration data).

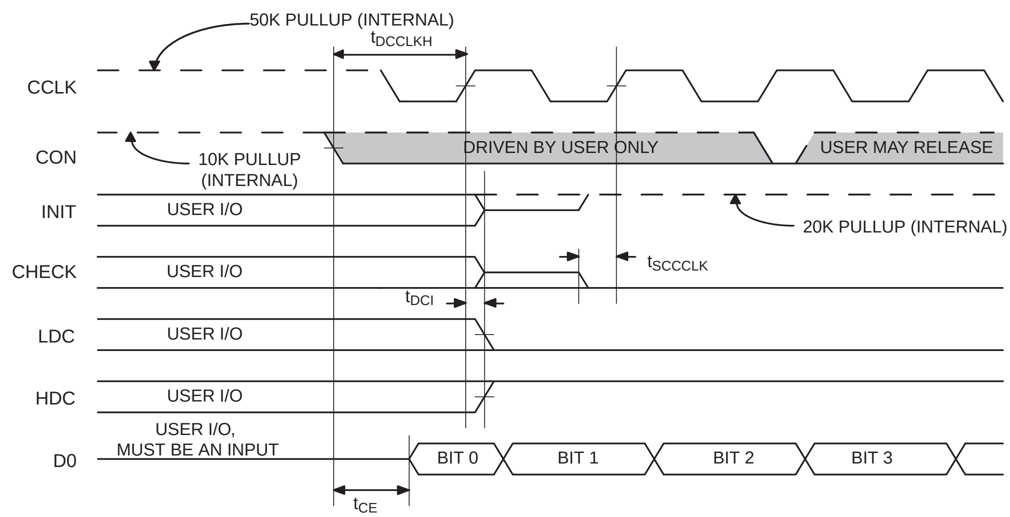
At the end of power-on-reset or manual reset, CON is not pulsed high. For the AT40K series devices, the either the RESET or INIT pin is tied to the Configurator OE/RESET pin, and CON is tied to the Configurator chip enable (Ce). Figure 7 shows the timing of the configuration interface after power-on-reset or manual reset and at the start of download. Figure 8 shows the timing of the configuration interface after manually initiating a configuration download from the idle state (without reset). Figure 9 shows the timing of the configuration interface at the end of configuration download. Table 10 shows the configuration timing parameters for these timing diagrams.

Figure 7. Master Serial Start of Auto-Configuration Download



Note: 1. Parameter t_{OE} is taken from the AT17 series data sheet.

Figure 8. Master Serial Start of Reconfiguration (without reset)



Notes:
1. INIT is an open drain pin during configuration downloads, so this pin must be driven only by an open drain driver. The pullup value should be properly chosen to allow the pin to be pulled high prior to the first rising edge of CCLK. Failure to do so will not cause the part to abort the download, but may cause the user confusion if the FPGA does drive the pin low.
2. Parameter t_{CE} is taken from the AT17 series data sheet.
3. For configuration interface inputs, t_{DCI} indicates the time for the User I/O to tristate.
4. Users must drive CON low for 3 rising edge of CCLK, and then should release.
5. During reconfiguration, when CON is driven low, the EEPROM begins driving immediately, but the FPGA will not claim the configuration interface until after the first rising edge of CCLK after CON goes low. The D_0 pin is a Dual Use I/O, but must remain an input in order for reconfiguration to operate properly. Failure to do so will cause contention between the Serial EEPROM and the FPGA when CON goes low.
6. The EEPROM's OE/RESET pin is wired to the INIT pin of the FPGA in the example wiring shown in Figure 6. The internal counters of the EEPROM are reset by a low pulse on the OE/RESET pin. The user must either load both the reconfiguration bitstream and the auto-configuration bitstream sequentially into the EEPROM, or pulse the OE/RESET pin low to reset the EEPROM and then reload the auto-configuration bitstream.

Figure 9. Master Serial End of Configuration Download

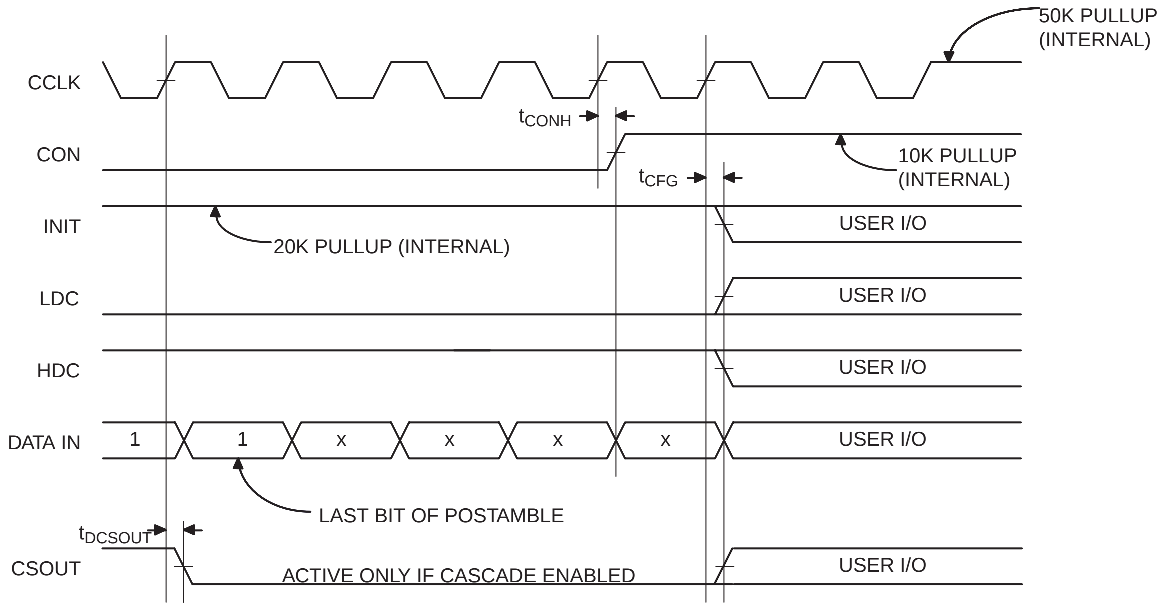


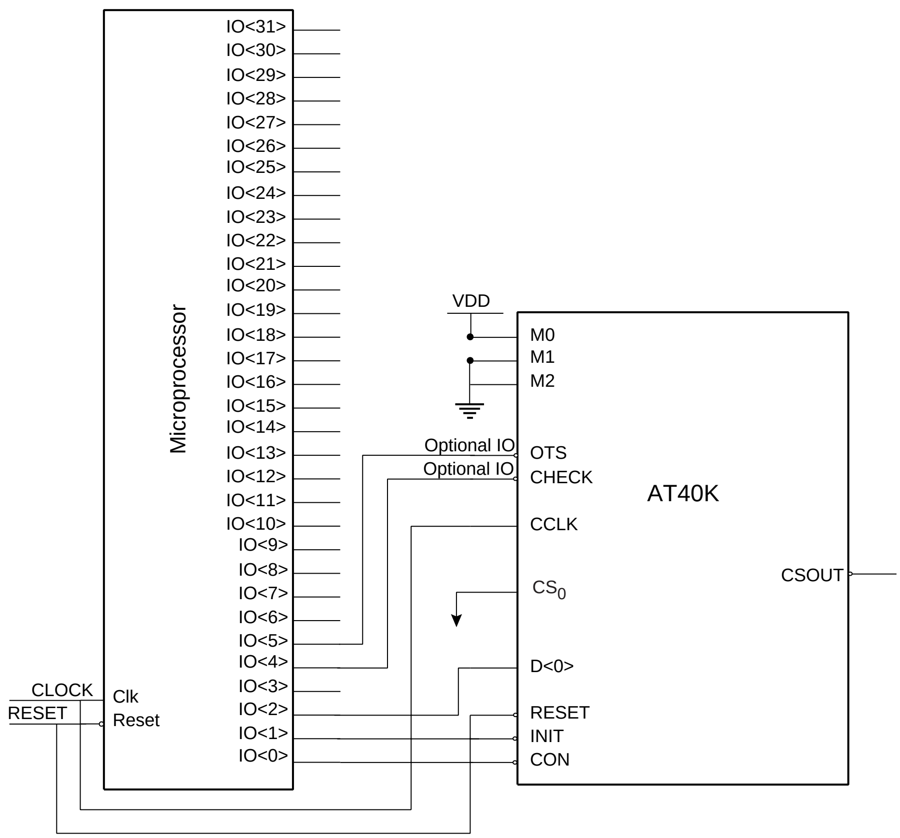
Table 10. Master Serial Configuration Timing Parameters @ 5V ± 10% Industrial/Commercial

Parameter	Description	Min	Typ	Max	Units
t_{PPCCLK}	Period of CCLK	0.6	1	1.6	µs
	2 MHz option	300	500	800	ns
	4 MHz option	150	250	400	ns
	8 MHz option	75	125	200	ns
t_{ICCLK}	Delay from rising edge of INIT after reset to first rising edge of CCLK	1.8	3	4.8	ns
t_{SCD}	Setup time for Data with respect to rising edge of CCLK	6	10	16	ns
t_{HCD}	Hold time for Data with respect to rising edge of CCLK	0	0	0	ns
t_{DCCLKH}	Delay from falling edge of CON to first rising edge of CCLK to start recognition.	0.6	1	1.6	µs
t_{SCCCLK}	Setup time for CHECK with respect to rising edge of CCLK at the start of a configuration download.	6	10	16	ns
t_{DCI}	Delay from rising edge of CCLK to activation of configuration interface pins at the start of recognition.	6	10	16	ns
t_{OE}	Delay from rising edge of OE/RESET of AT17 series Configurator EEPROM to data valid on Data Out of Configurator. Data taken from the AT17 series data sheet.			150	ns
t_{CE}	Delay from falling edge of CON to Data valid from AT17 series Configurator EEPROM. Data taken from the AT17 series data sheet.			45	ns
t_{CONH}	Delay from rising edge of CCLK to rising edge release of CON at the end of configuration. Timing is measured with a 50pg load and a 2.7K pullup resistor on CON. Actual time will depend on system loading of CON.		130		ns
t_{CFG}	Delay from rising edge of CCLK to the release of Dual Use pins to full user functionality.	6	10	16	ns
t_{DCSOUT}	Delay from rising edge of CCLK to CSOUT active at end of configuration.	6	10	16	ns

Mode 1: Slave Serial

Configuration Data Source:	Serial EEPROM, Microprocessor
Dedicated Configuration Pins:	RESET, CON, M_0, M_1, M_2, CCLK
Dual Use I/O:	D_0, INIT, LDC, HDC,
Optional Dual Use I/O:	CSOUT, CHECK, OTS

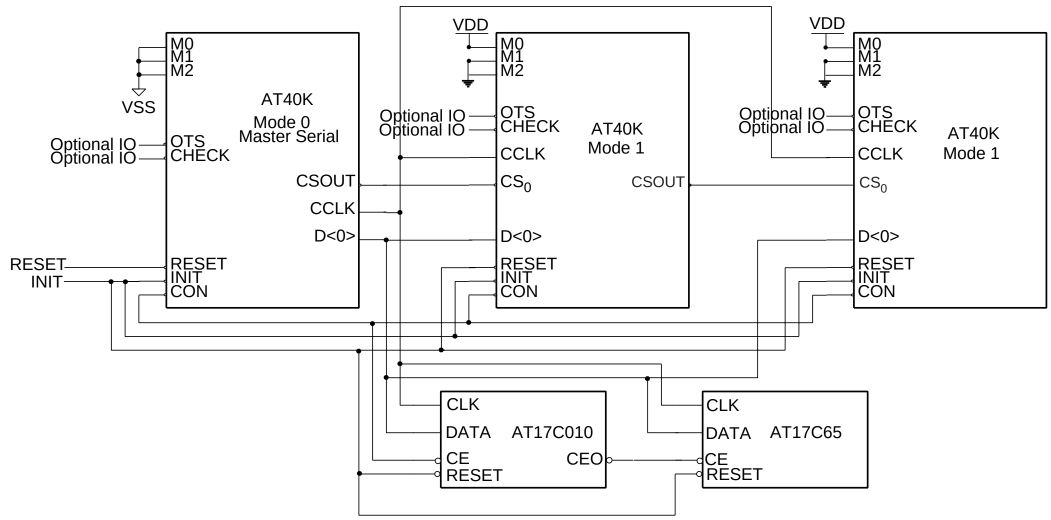
Figure 10. Standalone 1 Microprocessor System Application



A Mode 1 Slave Serial device is usually configured in a system whereby data comes either from a serial EEPROM or from the data port of a microprocessor. Figure 10 shows a typical system application with a microprocessor. Figure 11 shows a typical system application with a Mode 1 device serial EEPROM in a cascade chain with a Mode 0 device as the master in the chain.

In Mode 1, CCLK is driven by an external device, most often either a microprocessor or a Master Serial FPGA, in cascade mode. Like the Master Serial device, serial data is driven into the D_0 pin of the FPGA. To begin configuration, CON must be driven low. Once the bitstream is completed, CON is released by the FPGA, indicating the device is completely ready for user operation. Configuration time depends on the frequency of the external clock driving CCLK. The maximum frequency in which a Mode 1 device can be downloaded is 33 MHz. A full bitstream for the AT40K20 can be downloaded in only 4.6 ms (30 ns per bit of configuration data).

Figure 11. Cascade 0 11 Configurator System Application

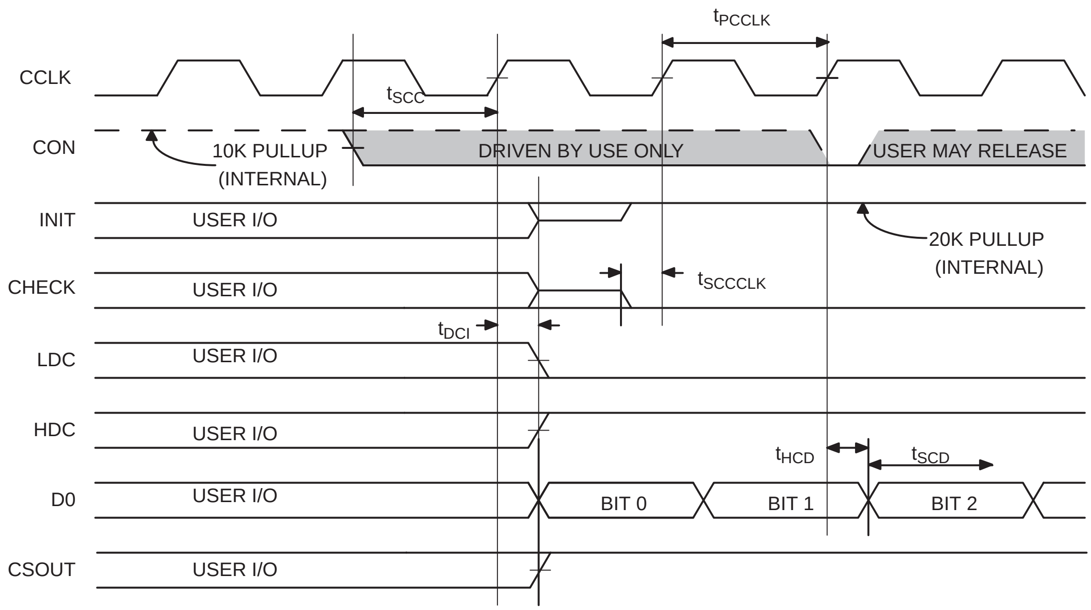


Note that all D_0 inputs for the FPGAs in the cascade chain are tied in parallel. The Master Serial device does not accept data intended for downstream devices and propagate it to the next device; instead, it simply passes a chip select downstream. Note that CSOUT of the upstream Master Serial device is connected to the CS_0 of the downstream device.

CS_0 is a Dual Use I/O pin is required as a chip select to enable the part to claim the configuration, so care must be taken by the user not to use the CS_0 pin in such a manner that the part may not be reconfigured. As an example, if the user programs CS_0 as an output driving high, then CS_0 cannot be lowered, and the part will never reconfigure without first either powering down or manually resetting. It is recommended therefore that for Slave Serial Mode, the user leave CS_0 as an input.

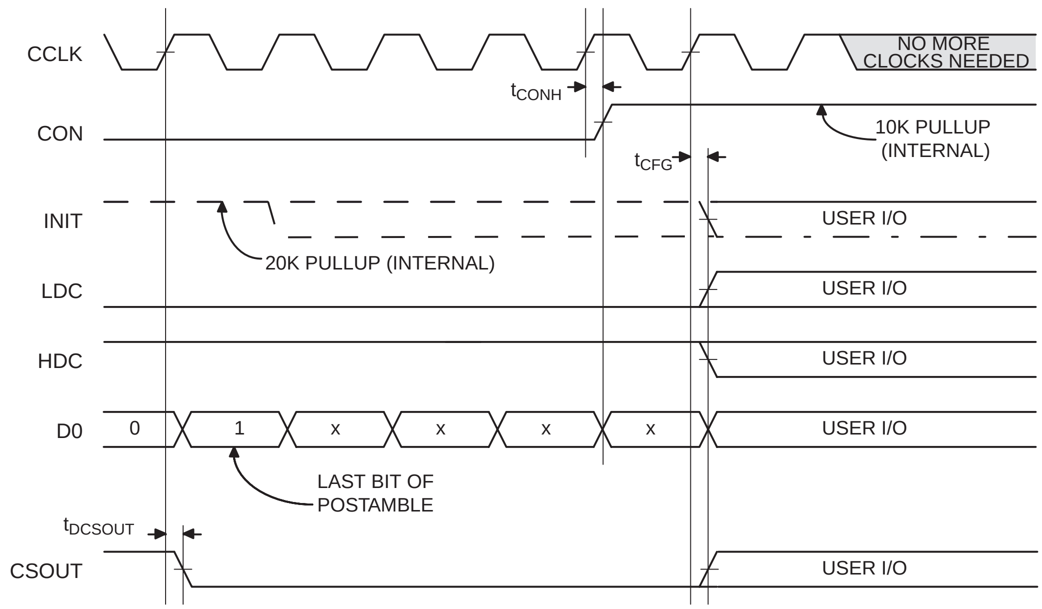
Figure 12 shows the timing of the configuration interface after manually initiating a configuration download from the idle state (without reset). Figure 13 shows the timing of the configuration interface at the end of configuration download. Figure 14 shows the timing of the configuration interface at the interface of the upstream and downstream devices in the cascade chain. Table 11 shows the configuration timing parameters pertaining to these timing diagrams.

Figure 12. Slave Serial Start of Configuration



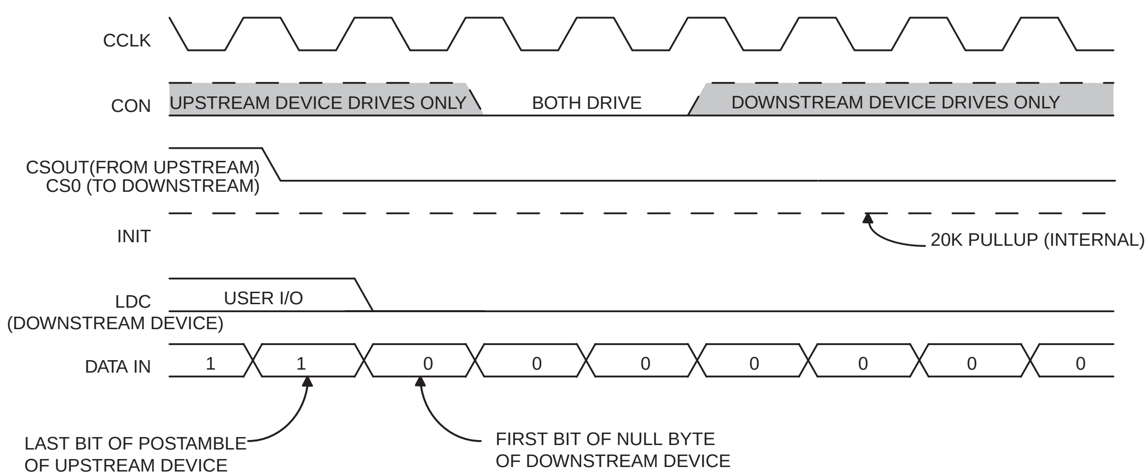
Notes:
1. INIT is an open drain pin during configuration downloads, this pin must be driven by only an open drain driver. The pullup value should be properly chosen to allow the pin to be pulled high prior to the first rising edge of CCLK. Failure to do so will not cause the part to abort the download, but may cause the user confusion if the FPGA does drive the pin low.
2. For configuration interface inputs, t_{DCI} indicates the time for the user I/O to tristate.
3. The pins CSOUT and CHECK are claimed by the configuration interface only if enabled by the control register. Both are enabled by default after power-on-reset or manual reset.
4. Users must drive CON low for 3 rising edges of CCLK, and then should release it.

Figure 13. Slave Serial End of Configuration Download



Notes:
1. For a configuration bitstream error, INIT is driven low on the second rising edge after the bitstream error is detected. In the above example, the "0" in the second to last bit of the postamble is inserted to produce the error shown. The proper value is "1". The error is shown for timing purposes only; under normal circumstances the bitstream download would terminate prematurely.
2. The pins CSOUT and CHECK are claimed by the configuration interface only if enabled by the control register. Both are enabled by default after power-on-reset or manual reset.

Figure 14. Serial Cascade Chain Interface Timing Diagram



Notes:
1. Cascade bitstream is formed by simple concatenation of upstream and downstream bitstreams.
2. INIT of upstream and downstream devices are tied together for above example.

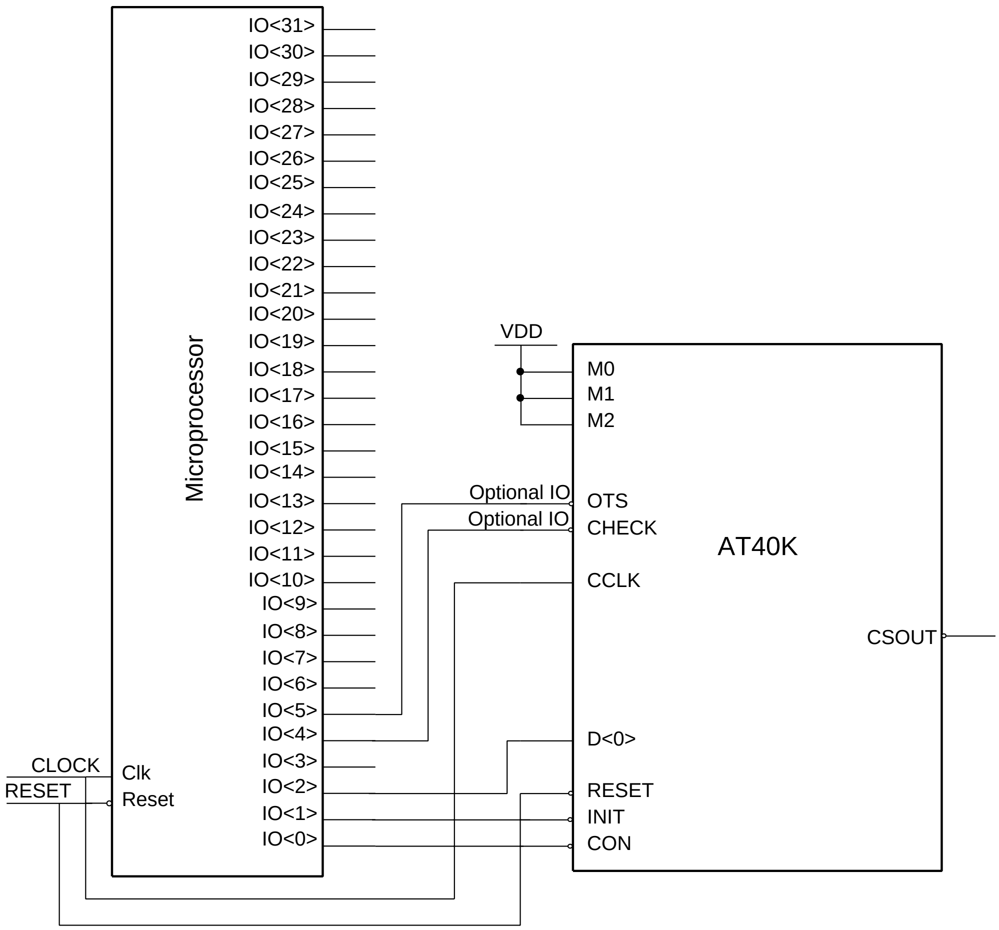
Table 11. Slave Serial Configuration Timing Parameters @ 5V ± 10% Industrial/Commercial Range

Parameter	Description	Min	Typ	Max	Units
t_{PPCCLK}	Period of CCLK for configuration downloads	30			ns
	Period of CCLK for configuration downloads with the check functions enabled	1000			ns
t_{SCC}	Setup time for CON and CSO with respect to rising edge of CCLK	6	10	16	ns
t_{SCD}	Setup time for data with respect to rising edge of CCLK	6	10	16	ns
t_{HCD}	Hold time for data with respect to rising edge of CCLK	0	0	0	ns
t_{SCCCLK}	Setup time for CHECK with respect to rising edge of CCLK at the start of a configuration download.	6	10	16	ns
t_{DCI}	Delay from rising edge of CCLK to activation of configuration interface at the start of reconfiguration	6	10	16	ns
t_{DCSOUT}	Delay from rising edge of CCLK to falling edge of CSOUT by upstream device during a cascade configuration	6	10	16	ns
t_{CONH}	Delay from rising edge of CCLK to rising edge release of CON at the end of configuration. Timing is measured with a 50pf load and a 2.7K pullup resistor on CON. Actual time will depend on system loading of CON.		130		ns
t_{CFG}	Delay from rising edge of CCLK to the release of dual use pins to full user functionality.	6	10	16	ns

Mode 7: Slave Serial

Configuration Data Source:	Serial EEPROM, Microprocessor
Dedicated Configuration Pins:	RESET, CON, M_0, M_1, M_2, CCLK
Dual Use I/O:	D_0, INIT, LDC, HDC
Optional Dual Use I/O:	CSOUT, CHECK

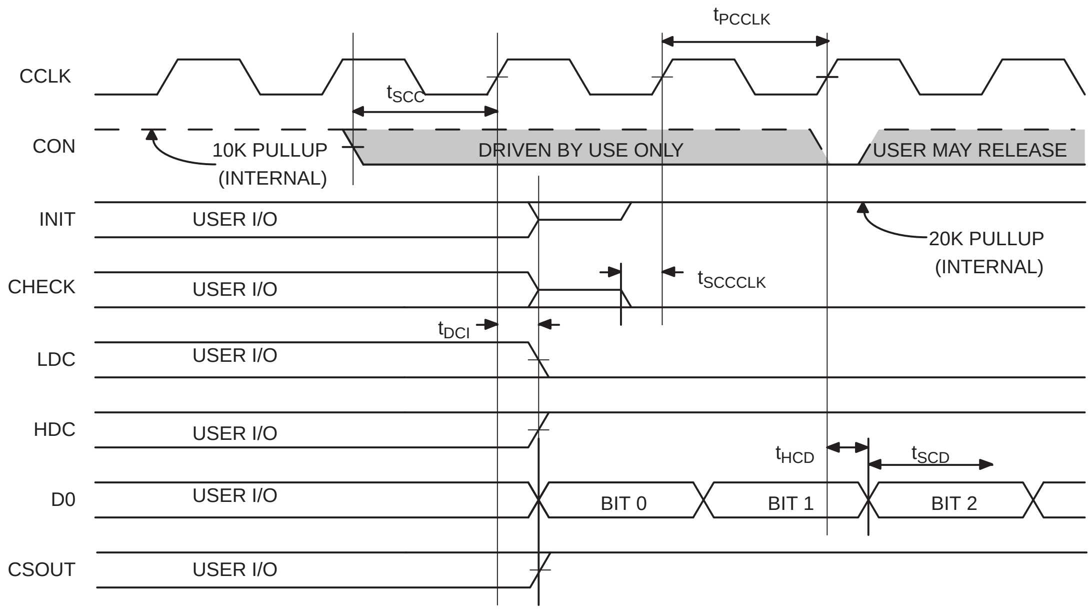
Figure 15. Standalone 7 Microprocessor System Application



A Mode 7 Slave Serial device is usually configured in a system whereby data comes either from a serial EEPROM or from the data port of a microprocessor. Figure 15 shows a typical system application with a microprocessor.

In Mode 7, CCLK is driven by an external device, most often either a microprocessor or a Master Serial FPGA, in cascade mode. Like the Master Serial device, serial data is driven into the D_0 pin of the FPGA. To begin configuration, CON must be driven low. Once the bitstream is completed, CON is released by the FPGA, indicating the device is completely ready for user operation. Configuration time depends on the frequency of the external clock driving CCLK. The maximum frequency in which a Mode 7 device can be downloaded is 33 MHz. A full bitstream for the AT40K20 can be downloaded in only 4.6 ms (30 ns per bit of configuration data).

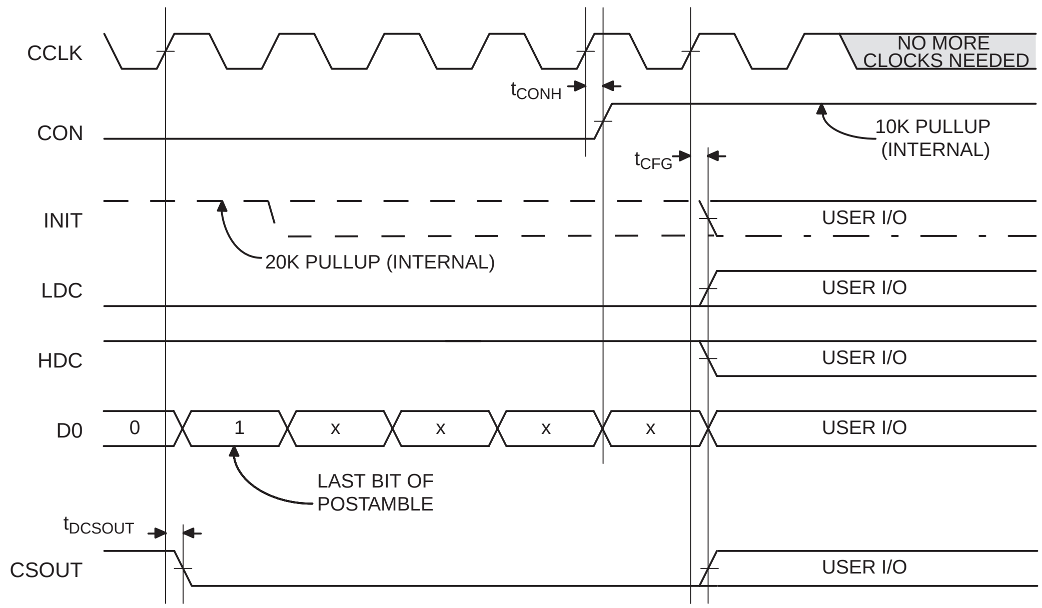
Figure 16. Slave Serial Start of Configuration



Notes:

1. INIT is an open drain pin during configuration downloads, this pin must be driven by only an open drain driver. The pullup value should be properly chosen to allow the pin to be pulled high prior to the first rising edge of CCLK. Failure to do so will not cause the part to abort the download, but may cause the user confusion if the FPGA does drive the pin low.
2. For configuration interface inputs, t_{DCI} indicates the time for the user I/O to tristate.
3. The pins CSOUT and CHECK are claimed by the configuration interface only if enabled by the control register. Both are enabled by default after power-on-reset or manual reset.
4. Users must drive CON low for 3 rising edges of CCLK, and then should release it.

Figure 17. Slave Serial End of Configuration Download



Notes: 1. For a configuration bitstream error, INIT is driven low on the second rising edge after the bitstream error is detected. In the above example, the "0" in the second to last bit of the postamble is inserted to produce the error shown. The proper value is "1". The error is shown for timing purposes only; under normal circumstances the bitstream download would terminate prematurely.

2. The pins CSOUT and CHECK are claimed by the configuration interface only if enabled by the control register. Both are enabled by default after power-on-reset or manual reset.

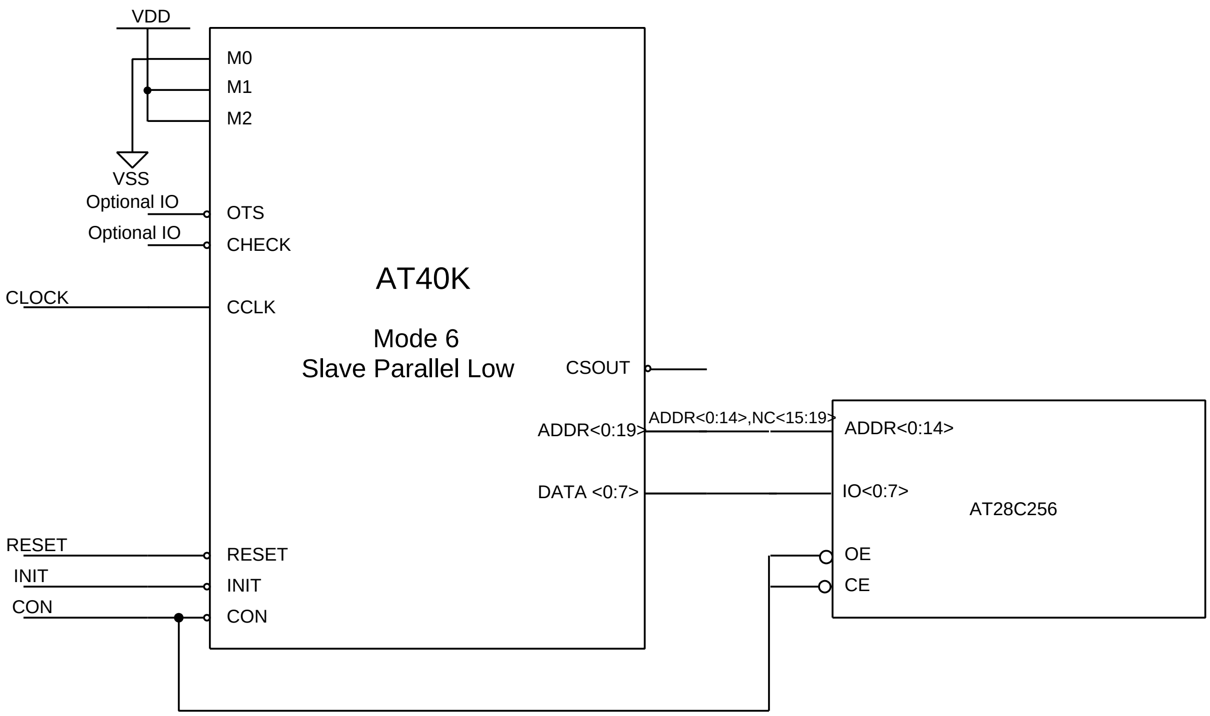
Table 12. Slave Serial Configuration Timing Parameters @ 5V ± 10% Industrial/Commercial Range

Parameter	Description	Min	Typ	Max	Units
t_{PPCCLK}	Period of CCLK for configuration downloads	30			ns
	Period of CCLK for configuration downloads with the check functions enabled	1000			ns
t_{SCC}	Setup time for CON with respect to rising edge of CCLK	6	10	16	ns
t_{SCD}	Setup time for data with respect to rising edge of CCLK	6	10	16	ns
t_{HCD}	Hold time for data with respect to rising edge of CCLK	0	0	0	ns
t_{SCCCLK}	Setup time for CHECK with respect to rising edge of CCLK at the start of a configuration download.	6	10	16	ns
t_{DCI}	Delay from rising edge of CCLK to activation of configuration interface at the start of reconfiguration	6	10	16	ns
t_{DCSOUT}	Delay from rising edge of CCLK to falling edge of CSOUT by upstream device during a cascade configuration	6	10	16	ns
t_{CONH}	Delay from rising edge of CCLK to rising edge release of CON at the end of configuration. Timing is measured with a 50pf load and a 2.7K pullup resistor on CON. Actual time will depend on system loading of CON.		130		ns
t_{CFG}	Delay from rising edge of CCLK to the release of dual use pins to full user functionality.	6	10	16	ns

Mode 6: Slave Parallel Up

Configuration Data Source:	Parallel EEPROM, EPROM, PROM
Dedicated Configuration Pins:	RESET, CON, M_0, M_1, M_2, CCLK
Dual Use I/O:	D_0:D_7, INIT, LDC, HDC, A_0:A_{19}
Optional Dual Use I/O:	CSOUT, CHECK, D_8:$D_{15,}$ OTS

Figure 18. Standalone 6 Parallel EEPROM System Application

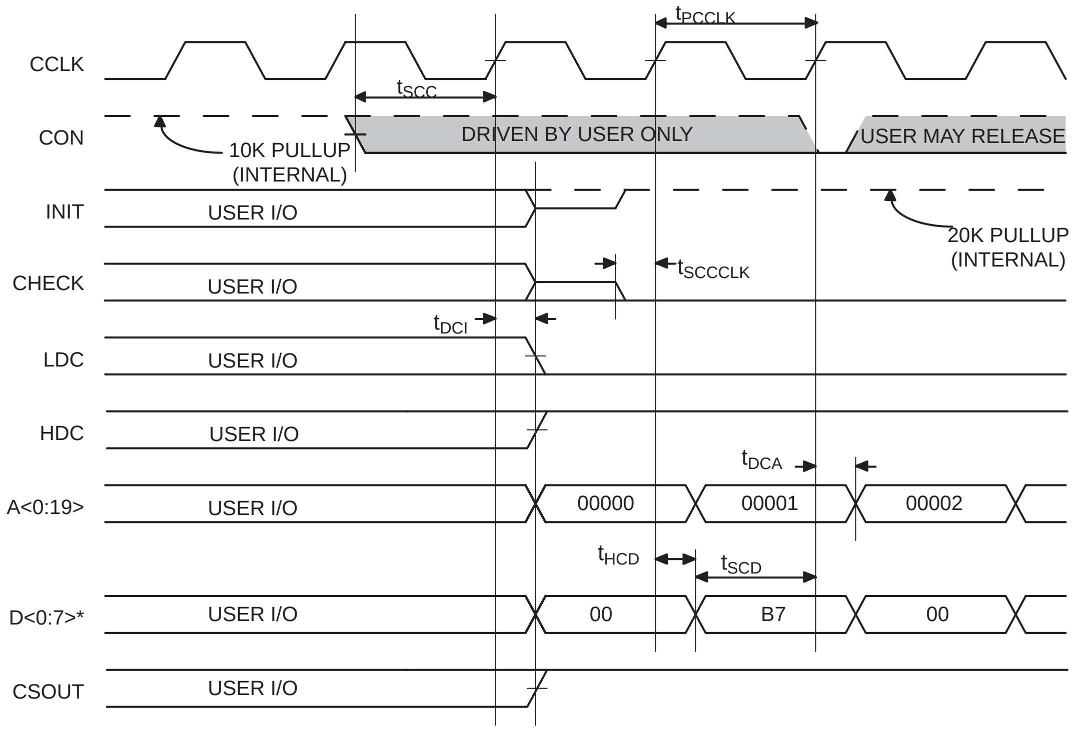


A Mode 6 Slave Parallel Up device is usually configured in a system whereby data comes from a parallel external memory, such as a PROM. Figure 18 shows a typical system application.

In Mode 6, CCLK is driven by an external device. On the rising edge of each CCLK, an address is supplied by the FPGA to an external memory, and parallel data is clocked into the FPGA. To begin configuration, CON is driven low. There is no chip select for Mode 6, since it is always configured as the most upstream device in a cascade chain. Once the bitstream is completed, CON is released by the FPGA, indicating the device is completely ready for user operation. Configuration time depends on the frequency of the external clock driving CCLK. The maximum frequency in which a Mode 6 device can be downloaded is 33 MHz. A full bitstream for the AT40K20 can be downloaded in only 0.30 ms (30 ns per word of configuration data).

Figure 19 shows the timing of the configuration interface after manually initiating a configuration download from the idle state (without reset). Figure 20 shows the timing of the configuration interface at the end of configuration download. Table 13 shows the configuration timing specifications pertaining to these timing diagrams.

Figure 19. Slave Parallel Up Start of Configuration

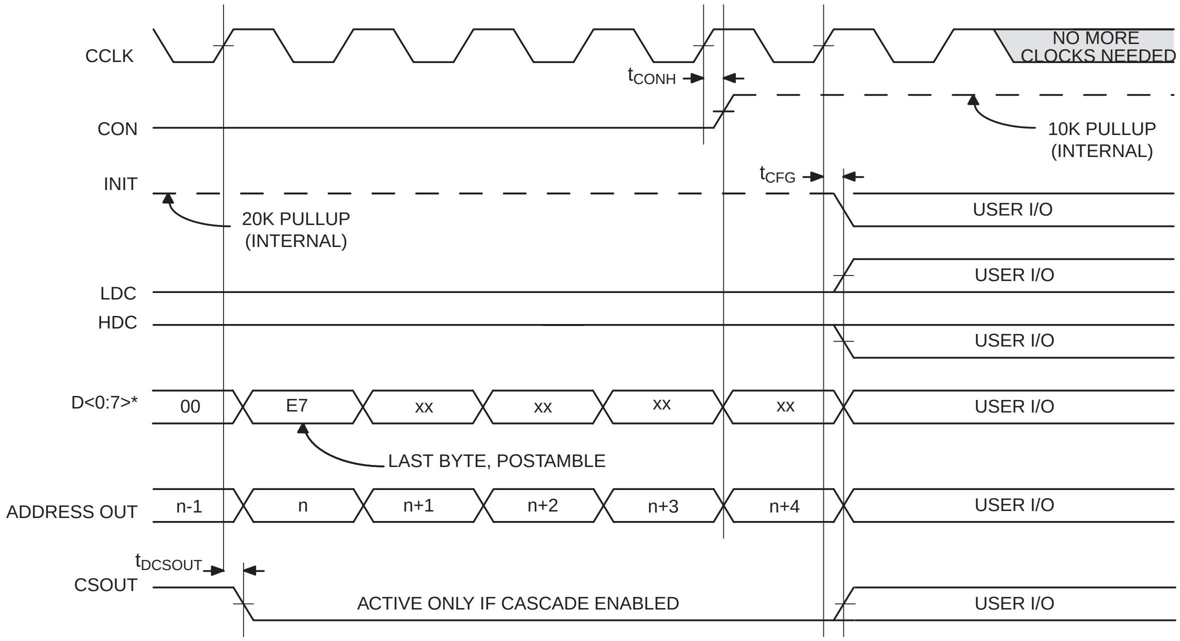


Notes:

1. INIT is an open drain pin during configuration downloads, this pin must be driven by only an open drain driver. The pullup value should be properly chosen to allow the pin to be pulled high prior to the first rising edge of CCLK. Failure to do so will not cause the part to abort the download, but may cause the user confusion if the FPGA does drive the pin low.
2. For configuration interface inputs, t_{DCI} indicates the time for the user I/O to tristate.
3. The pins CSOUT and CHECK are claimed by the configuration interface only if enabled by the control register. Both are enabled by default after power-on-reset or manual reset.
4. Users must drive CON low for 3 rising edges of CCLK, and then should release.

* Data can also be loaded D<0:15> as a 16-bit word.

Figure 20. Slave Parallel Up End of Configuration Download



Notes:
1. The pins CSOUT and CHECK are claimed by the configuration interface only if enabled by the control register. Both are enabled by default after power-on-reset or manual reset.
2. The Address up counter counts 4 addresses beyond the postamble address, which is the last byte of the bitstream.

* Data can also be loaded D<0:15> as a 16-bit word.

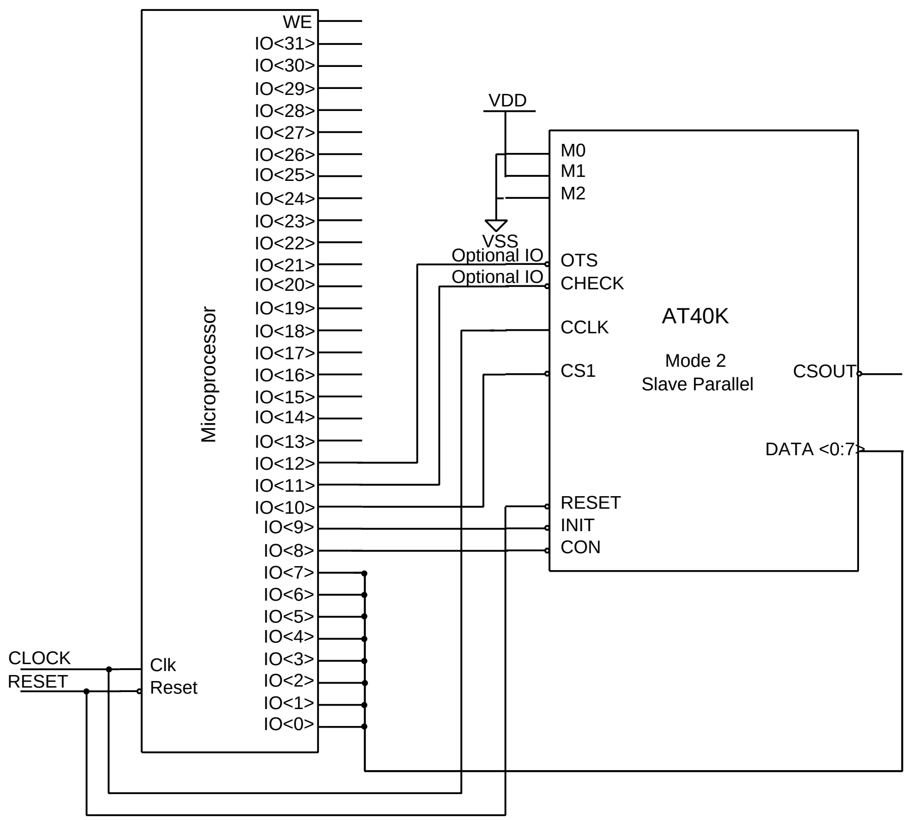
Table 13. Slave Parallel Up Configuration Timing Parameters @ 5V ± 10% Industrial/Commercial Range

Parameter	Description	Min	Typ	Max	Units
t_{PCCLK}	Period of CCLK for configuration downloads	30			ns
	Period of CCLK for configuration downloads with the check function enabled	1000			ns
t_{SCC}	Setup time for CON with respect to rising edge of CCLK	6	10	16	ns
t_{DCA}	Delay from rising edge of CCLK to valid address out	3	13	19	ns
t_{SCD}	Setup time for data with respect to rising edge of CCLK	6	10	16	ns
t_{HCD}	Hold time for data with respect to rising edge of CCLK	0	0	0	ns
t_{SCCCLK}	Setup time for CHECK with respect to rising edge of CCLK at the start of a configuration download.	6	10	16	ns
t_{DCI}	Delay from rising edge of CCLK to activation of configuration interface at the start of recognition.	6	10	16	ns
t_{DCSOUT}	Delay from rising edge of CCLK to falling edge of CSOUT by upstream device during a cascade configuration	6	10	16	ns
t_{CONH}	Delay from rising edge of CCLK to rising edge release on CON at the end of configuration. Timing is measured with a 50pf load and a 2.7K pullup resistor on CON. Actual time will depend on system loading of CON.		130		ns
t_{CFG}	Delay from rising edge of CCLK to the release of Dual Use pins to full user functionality.	6	10	16	ns

Mode 2: Slave Parallel

Configuration Data Source:	Microprocessor, Parallel EEPROM, EPROM, PROM
Dedicated Configuration Pins:	RESET, CON, M_0, M_1, M_2, CCLK
Dual Use I/O:	D_0:D_7, INIT, LDC, HDC, CS_1, OTS
Optional Dual Use I/O:	CSOUT, CHECK, D_8:D_{15}

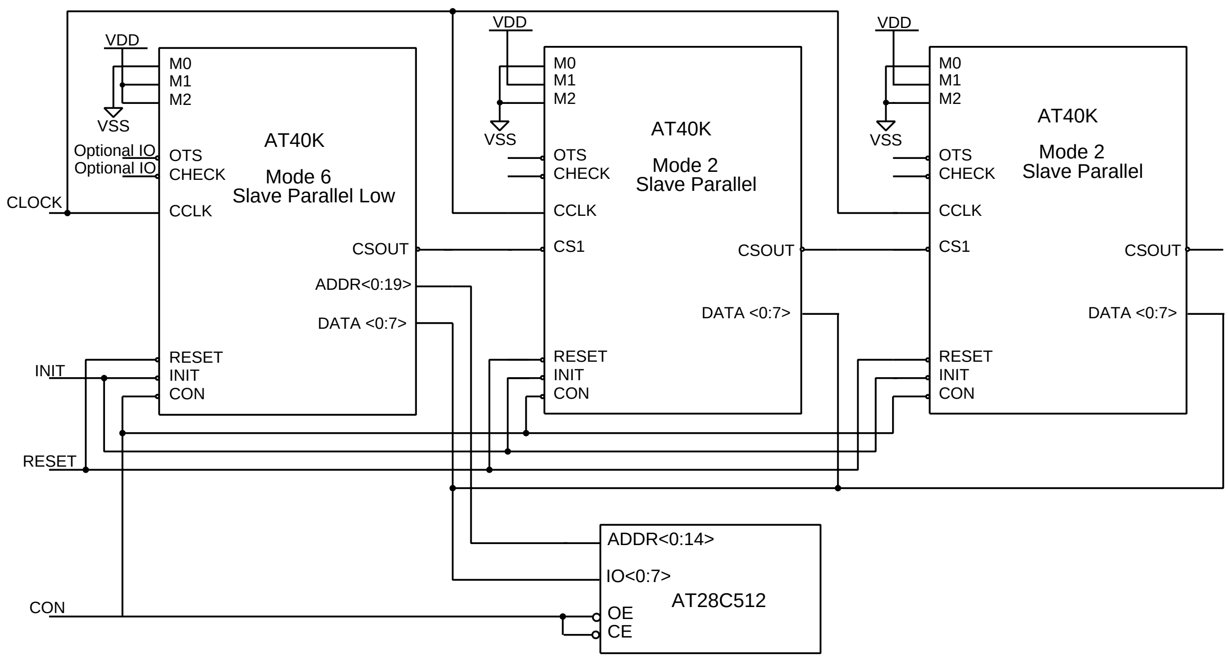
Figure 21. Standalone 2 Microprocessor



A Mode 2 Slave Parallel device is usually configured in a system in one of two ways. The first is a standalone or cascade scheme whereby data comes from a microprocessor. Figure 21 shows this typical system application. The other is a cascade scheme where the data is driven by a parallel PROM, and the FPGA is usually downstream from a Mode 6 device. Figure 22 shows a 6-2-2 cascade system application.

In Mode 2, CCLK is driven by an external device. On the rising edge of each CCLK, parallel data is clocked into the FPGA. To begin configuration, CON and the chip select (CS_1) must be driven low. Once the bitstream is completed, CON is released, indicating the device is completely ready for user operation. Configuration time depends on the frequency of the external clock driving CCLK. The maximum frequency in which a Mode 2 device can be downloaded is 33 MHz. A full bitstream for the AT40K20 can be downloaded in only 0.30 ms (30 ns per word of configuration data). Any bitstream errors cause the INIT pin to drive low. Figure 23 shows the timing of the configuration interface after manually initiating a configuration download from the idle state (without reset). Figure 24 shows the timing of the configuration interface at the end of configuration download. Figure 25 shows the timing of the configuration interface at the interface of the upstream and downstream devices in the cascade chain. Table 14 shows the configuration timing specifications pertaining to these timing diagrams.

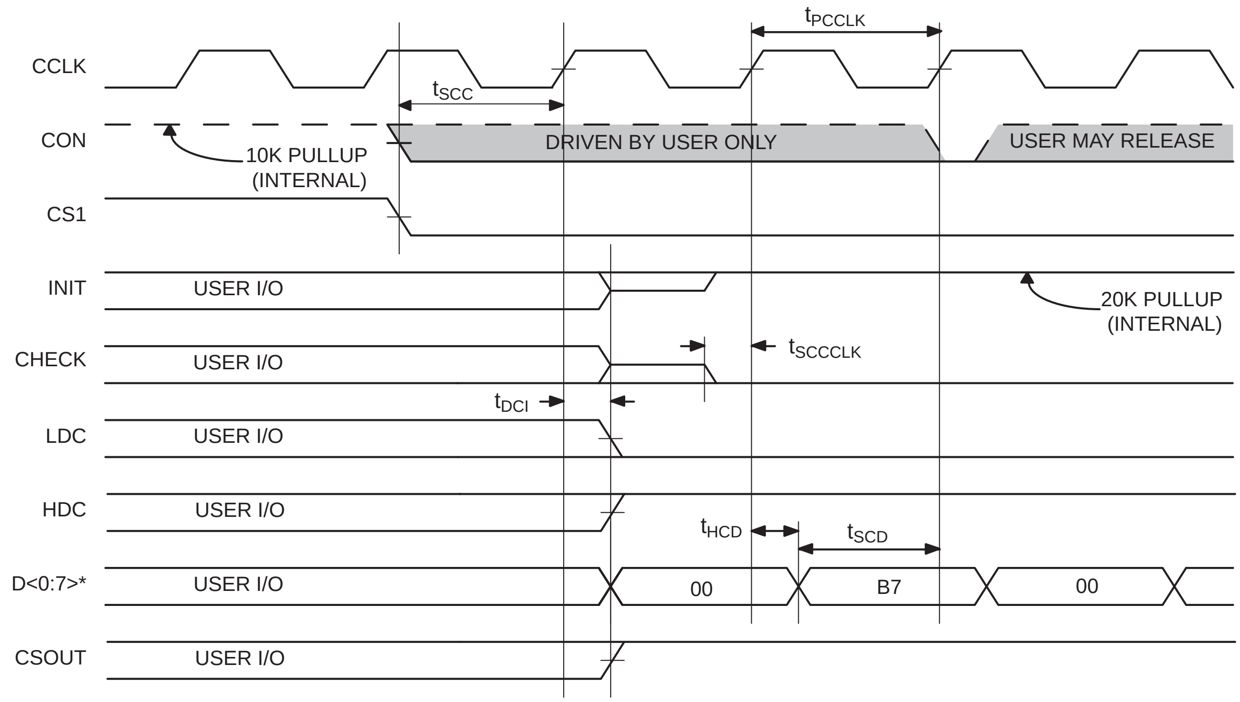
Figure 22. Cascade 6 2 2 Parallel EEPROM



Note that all D_0:D_7 inputs for the FPGAs in the cascade chain are tied in parallel. The upstream device does not accept data intended for downstream devices and propagate it to the next device; instead, it simply passes a chip select downstream. Note that CSOUT of the upstream device is connected to the CS_1 of the downstream device.

CS_1 is a Dual Use I/O pin required as a chip select to enable the part to claim the configuration interface. Care must be taken by the user not to use the CS_1 pin in such a manner that the part may not be reconfigured. As an example, if the user programs CS_1 as an output driving high, then CS_1 cannot be lowered, and the part will never reconfigure without first either powering down or manually resetting. It is recommended therefore that for Slave Parallel mode, the user leave CS_1 as an input.

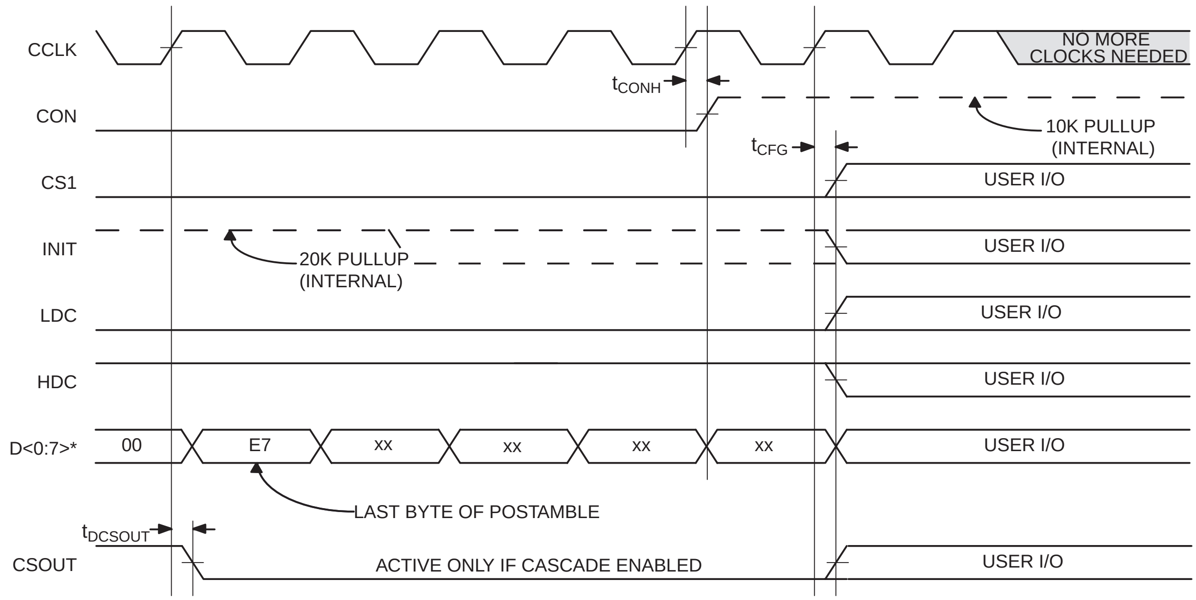
Figure 23. Slave Parallel Start of Configuration



Notes:
1. INIT is an open drain pin during configuration downloads, so this pin must be driven by only an open drain driver. The pullup value should be properly chosen to allow the pin to be pulled high prior to the first rising edge of CCLK. Failure to do so will not cause the part to abort the download, but may cause the user confusion if the FPGA does drive the pin low.
2. For configuration interface inputs, t_{DCI} indicates the time for the user I/O to tristate.
3. The pins CSOUT and CHECK are claimed by the configuration interface only if enabled by the control register. Both are enabled by default after power-on-reset or manual reset.
4. Users must drive CON low for 3 rising edges of CCLK, and then should release.

* Data can also be loaded D<0:15> as a 16-bit word.

Figure 24. Slave Parallel End of Configuration Download

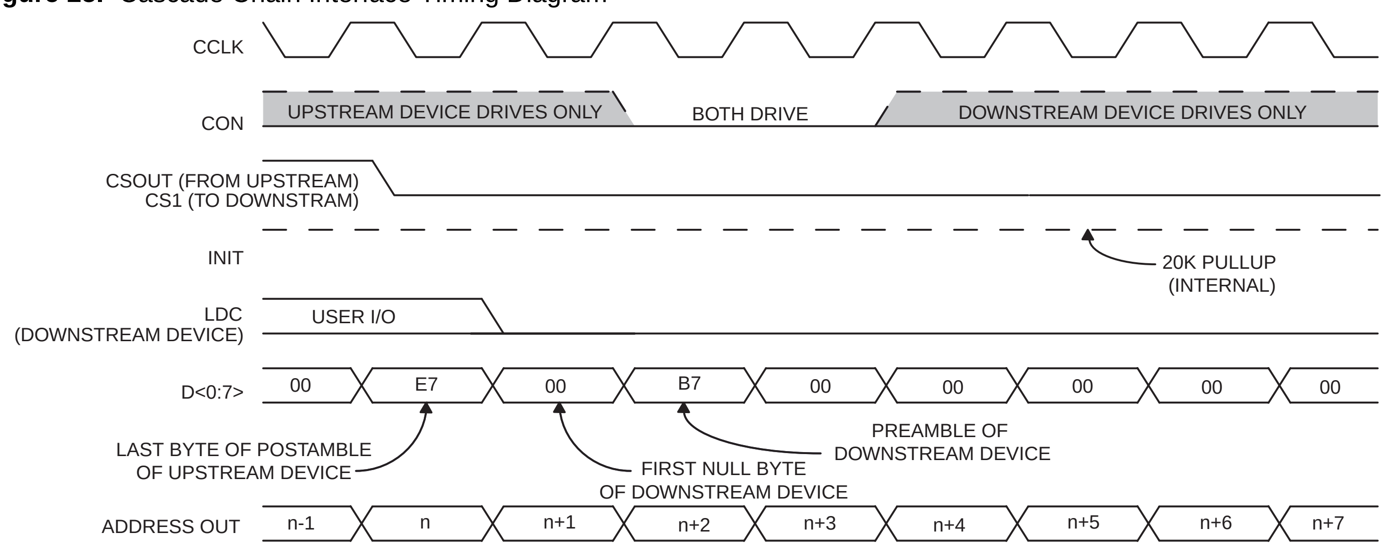


Notes: 1. For a configuration bitstream error, INIT is driven low on the second rising edge after the bitstream error is detected. In the above example, the "00" in the second to last bit of the postamble is inserted to produce the error shown. The error is shown for timing purposes only; under normal circumstances the bitstream download would terminate prematurely.

2. The pins CSOUT and CHECK are claimed by the configuration interface only if enabled by the control register. Both are enabled by default after power-on-reset or manual reset.

* Data can also be loaded D<0:15> as a 16-bit word.

Figure 25. Cascade Chain Interface Timing Diagram



Notes: 1. Cascade bitstream is formed by simple concentration of upstream and downstream bitstreams.

2. INIT of upstream and downstream devices are tied together for above example.

* Data can be driven D<0:15> as a 16-bit word.

Table 14. Slave Parallel Configuration Timing Parameters @ 5V ± 10% Industrial/Commercial Range

Parameter	Description	Min	Typ	Max	Units
t_{PCCLK}	Period of CCLK for configuration downloads	30			ns
	Period of CCLK for configuration downloads with the check function enabled	1000			ns
t_{SCC}	Setup time for CON and CS_1 with respect to rising edge of CCLK	6	10	16	ns
t_{SCD}	Setup time for data with respect to rising edge of CCLK	6	10	16	ns
t_{HCD}	Hold time for data with respect to rising edge of CCLK	0	0	0	ns
t_{SCCCLK}	Setup time for CHECK with respect to rising edge of CCLK at the start of a configuration download.	6	10	16	ns
t_{DCI}	Delay from rising edge of CCLK to activation of configuration interface at the start of reconfiguration	6	10	16	ns
t_{DCSOUT}	Delay from rising edge of CCLK to falling edge of CSOUT by upstream device during a cascade configuration	6	10	16	ns
t_{CONH}	Delay from rising edge of CCLK to rising edge release of CON at the end of configuration. Timing is measured with a 50pf load and a 2.7K pullup resistor on CON. Actual time will depend on system loading of CON.		130		ns
t_{CFG}	Delay from rising edge of CCLK to the release of dual use pins to full user functionality.	6	10	16	ns

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