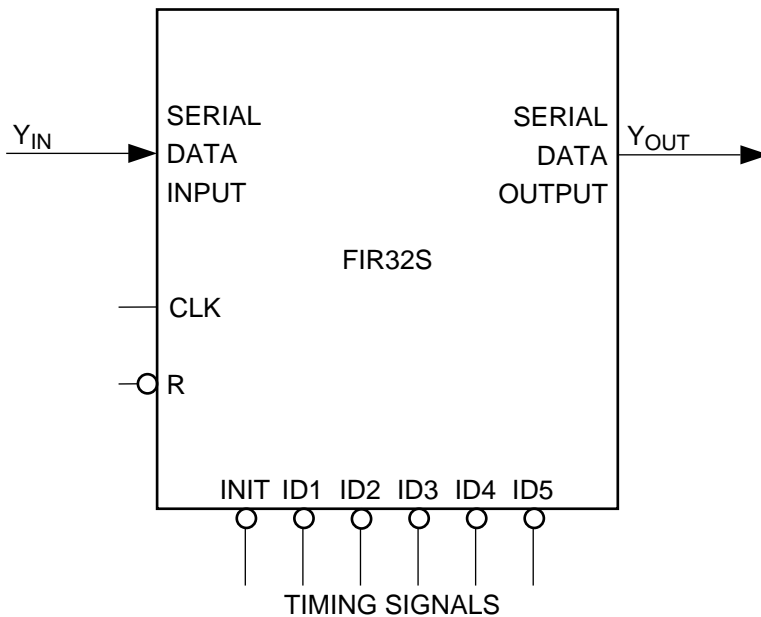


Symmetrical 32-tap FIR Filter Macro (FIR32S)



- Variable coefficient-type design
- Coefficient update in real-time via partial dynamic reconfiguration
- Bit-Serial Digital Signal Processing
- 5M-Samples/second – maximum sample rate

Design Statistics for “FIR32S”

Utilization Summary	Utilized
Speed (MHz)	74.0
Delay (ns)	13.5
Cells	2184
Size (x * y)	42 x 64
Gates (ASIC)	9400
Power (mA/MHz) (80% duty cycle)	2.62

The symmetrical 32-tap FIR filter macro is constructed by cascading the symmetrical 8-tap FIR filter hard macro (FIR8S). The FIR8S macro is designed to be cascaded by breaking the delay-line between the 4th and 5th taps and connecting to the input and cascade outputs, respectively, of the next macro block. The outputs from the filter macros are summed by additional carry-save adder (CSADDI) stages. In the final macro stage, the cascade tap input/outputs are connected together.

The coefficients are stored as constant cells in the Atmel AT6000 FPGA architecture. This provides the compact and

efficient storage of a fixed-coefficient scheme but is variable in real-time through the use of Cache-Logic™ (dynamic partial reconfiguration of the FPGA). Any one or more of the coefficients can be modified by sending the appropriate bit-stream(s) to the FPGA. While the updates occur, the filter continues to operate undisturbed as does the rest of the circuitry in the array. This is another unique benefit of Atmel FPGAs.

Control of the filter is achieved by generating an initialization signal at each new sample time. This single clock-cycle wide pulse is delivered to the filter as the



FPGA Digital Filter

Application Note



LSB of each sample is presented to the pre-add stages. This signal insures that the carry signals are reset at the beginning of each process cycle. Delayed versions of this signal are input to the multipliers and serial column adder, initializing each carry-save adder in the SPMs and the adder tree. As additional FIR8S stages are cascaded, additional initialization pulses are derived by adding stages to the control shift register.

QuickChange

In support of the CacheLogic capability, Atmel has developed QuickChange™, a multi-parameter specification software tool that allows the designer to interactively specify multiple parameters for digital filters, convolvers, and other

compute-oriented hardware. After completing the design with an initial set of parameters, the designer simply invokes QuickChange from the Atmel design environment. QuickChange searches the design for filter coefficients or other parameters, logically groups them and displays them in a graphical user-interface. The designer can then specify as many replacement sets of parameters as desired. The QuickChange tool then generates the FPGA bitstreams for each new parameter or sets of parameters. These small bitstream files, called “windowed” bit-streams, partially reconfigure the FPGA without affecting the operation of existing logic.

