Modeling Device Power Consumption

Field Programmable Gate Array

Application Note

Introduction

The following provides a simple method for modeling the active and static power consumption of a AT6005 design.

Active Power Consumption

Active power consumption is a function of the distribution of resources in a design and the number of nets switching each second. The distribution of resources is calculated by counting the instances in the design database. The Integrated Development System (IDS) reports this information in the list files generated by programs like placement, routing and bit stream generation. The switching of some nets, like clock signals and flip-flop outputs, is determined by clock frequency and can be tabulated exactly. The switching of other nets, especially combinatorial logic, is input-dependent and not solely determined by the clock. As a result, the activity of these nodes can only be estimated. Combinatorial signals are typically half as active as the clock. Test vectors representative of actual design operation can give a more accurate calculation. ViewLogic's "activity" command calculates the number of active nodes in a design during logic simulation.

The equation for active power consumption is as follows:

$$\text{POWER} = \text{Frequency} \times (\text{Aa} \times \text{Ka} \times \text{Na} + \text{Ab} \times \text{Kb} \times \text{Nb} + \text{Al} \times \text{Kl} \times \text{Nl} + \text{Ax} \times \text{Kx} \times \text{Nx} + \text{Ac} \times \text{Kc} \times \text{Nc} + \text{Kg} \times \text{Ng} + \text{Ai} \times \text{Ki} \times \text{Ni} + \text{Ao} \times \text{Ko} \times \text{No}) \times V_{CC}$$

The N coefficients represent the design resources reported by the IDS:

- *Na* number of A-type nets used (individual cell function is not important)
- *Nb* number of B-type nets used (individual cell function is not important)
- *Nl* number of local-bus type nets used
- *Nx* number of express-bus type nets used
- *Nc* number of clock columns used
- *Ng* 1 if global clock is used
- *Ni* number of I/O inputs
- *No* number of I/O outputs with no output load used

The A coefficients represent the estimated activity of combinatorial logic.

The K coefficients represent the weighting factor of each component:

Ka = 2 µA/MHz *Kb = 2 µA/MHz*
Kl = 4 µA/MHz *Kx = 3 µA/MHz*
Kc = 100 µA/MHz *Kg = 200 µA/MHz*
Ki = 4 µA/MHz *Ko = 60 µA/MHz*

The amount of activity possible is based on the number of each cell type used. The AT6005 has the following available:

Na = 3136 *Nb = 3136*
Nl = 1568 *Ne = 1568*
Nc = 56 *Ng = 1*
Ki = 64 (84-pin) or 108 (132-pin)
Ko = 64 (84-pin) or 108 (132-pin)

If every node were active at 10 MHz, the device would use about 293 mA of current (1466 mW).

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A more typical example would be:

Na = 2000 *Ab = 2000*
Al = 1200 *Ae = 700*
Ac = 27 *Ag = 1*
Ki = 54 *Ko = 54*

Yielding an active power consumption of:

$$\begin{aligned}\text{POWER} &= 2000 \times 0.5 \times 2 + 2000 \times 0.5 \times 2 + 1200 \times 0.5 \times 4 \\ &+ 300 \times 0.5 \times 3 + 27 \times 1 \times 100 + 1 \times 1 \times 200 + 54 \\ &\times 0.5 \times 4 + 54 \times 0.5 \times 60 \\ &= 11.5 \text{ mA/MHz}\end{aligned}$$

Or, 115 mA at 10 MHz (575 mW at 10 MHz).

Quiescent Power Consumption

The AT6005 is a CMOS device. Once programmed, the SRAM used to store the configuration requires no static power. The programmable interconnect points use complementary CMOS pass gates; this insures that all signals eventually reach V_{CC} or GND and dissipate no static power. There are no passive pull-ups on any internal nodes. Unused nets and buses are tied to V_{CC} and GND, and dissipate no power. Tri-states without active drivers dissipate some static power, but this is easily avoided.

Static power dissipation, measured after power-up in modes 1, 2, 3, or 6, but before programming, is 2 mA. After power-up, the device is programmed as a large array of registers with no inputs connected. Modes 4 and 5 generate a clock output signal. The power dissipation of modes 4 and 5 is 2 mA plus the power dissipation of the CCLK output driver, which is a function of the pin's loading capacitance. CCLK is typically 1 MHz.

The primary source of static power dissipation is not the core array, but the SRAM configuration circuitry. It has two blocks which consume static power – a power supply voltage monitor and an internal oscillator. The voltage monitor is used to initiate reboot when V_{CC} is first applied or when V_{CC} goes below a critical voltage. The monitor can not be disabled. The internal oscillator can be turned off by setting the B5 bit in the configuration register. With B5 set, the AT6005 dissipates less than 900 µA static power (Table 1).

Power consumption calculation is performed automatically by the Integrated Design System.

Table 1. AT6005 Static Power Dissipation

		Min	Typ	Max
I_{CC1}	Modes 1, 2, 3, 6 Measured after reboot			2 mA
I_{CC1}	Modes 4, 5 With 50p load on CCLK		5 mA	
I_{CC2}	Modes 1, 2, 3, 4, 5, 6 B5 Bit set with CONN = CSN = V_{CC}		900 µA	

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