



## Configuration Compression Algorithm

### Introduction

AT6000 Series FPGAs are SRAM-based and can be reconfigured to perform different applications in a system. Formulas show how the act of reconfiguration affects system performance. A proprietary compression algorithm reduces reconfiguration time and improves system performance. This algorithm is incorporated into the bit stream generation software provided in the Integrated Development System.

### Description

Two factors determine configuration time – the frequency of the configuration clock and the configuration mode used.

The configuration clock, CCLK, regulates the loading of data. The higher the clock frequency, the faster data is loaded. Modes 4 and 5 use an internally supplied clock that runs at only 1 MHz. The other modes employ a user-supplied clock. The user-supplied clock can run as fast as 10 MHz.

Of the two kinds of configuration, serial and parallel, parallel configuration is faster. Serial configuration loads one bit per clock cycle, while parallel configuration loads eight bits per clock cycle. As a result, a serial configuration mode takes eight times longer to load a bit stream. Table 1 gives equations that determine configuration times for the AT6002 and AT6005.

Partial configuration is naturally faster than full configuration. A configuration compression algorithm, supplied with Atmel's development system, filters full-configuration data to produce a partial configuration bit stream. The bit stream produced by the compression algorithm only programs memory that is different from the present configuration. On power-up, for example, each cell in the array is a zero. The compression algorithm can remove all the zeros from the bit stream to be used after power-up – in some cases reducing the size of the bit stream by as much as 50%.

This reduction provides a proportional reduction in configuration time, as shown in Table 1.

**Table 1.** Configuration Timing Equations

<b>Without Compression</b>	<b>AT6002</b>	<b>AT6005</b>
Serial	$2678 \times 8 \times 1/\text{Frequency}$	$8077 \times 8 \times 1/\text{Frequency}$
Parallel	$2678 \times 1/\text{Frequency}$	$8077 \times 1/\text{Frequency}$
<b>With Compression</b>	<b>AT6002</b>	<b>AT6005</b>
Serial	$(1 - \% \text{ Reduction}) \times 2678 \times 8 \times 1/\text{Frequency}$	$(1 - \% \text{ Reduction}) \times 8077 \times 8 \times 1/\text{Frequency}$
Parallel	$(1 - \% \text{ Reduction}) \times 2678 \times 1/\text{Frequency}$	$(1 - \% \text{ Reduction}) \times 8077 \times 1/\text{Frequency}$

## Field Programmable Gate Array

## Application Note





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