



Digital Frequency/Phase Comparator (DFPC)

Introduction

The AT6000 Series field programmable gate array (FPGA) lets the designer implement a digital frequency/phase comparator (DFPC) that interfaces to a voltage controlled oscillator (VCO).

Description

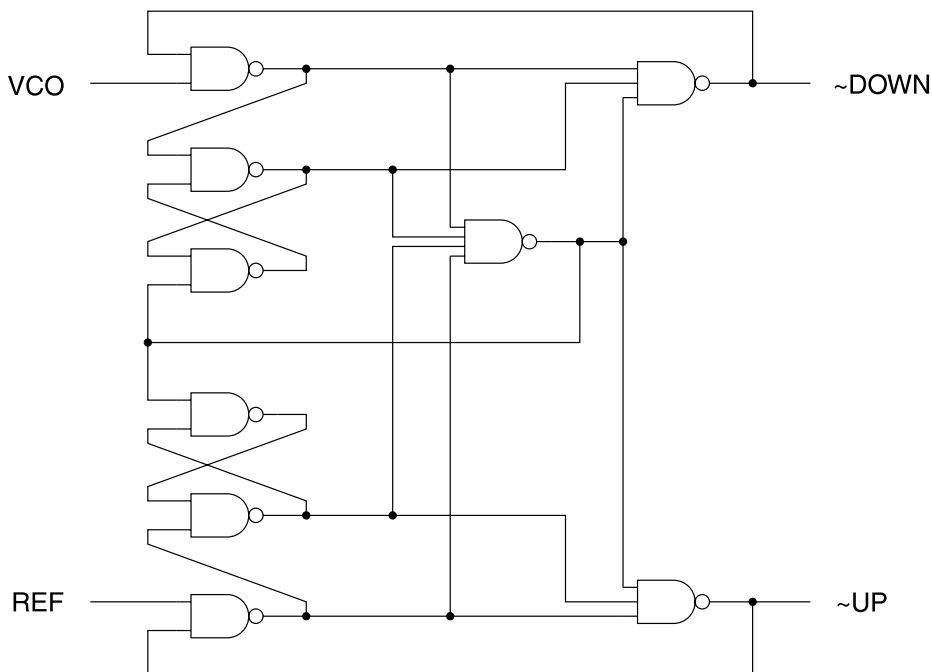
The DFPC has two periodic input signals, a reference frequency of some desired value and a variable frequency

from the VCO. Two output signals from the DFPC, ~UP and ~DOWN, control the VCO. These two signals change the VCO output frequency so as to match the reference frequency entering the DFPC. Once the reference and the variable signals have the same phase and frequency, the DFPC continues to make small adjustments to the VCO frequency to maintain the match.

Field Programmable Gate Array

Application Note

Figure 1. Digital Frequency/Phase Comparator Circuit



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Figure 3. DFPC Test Circuits

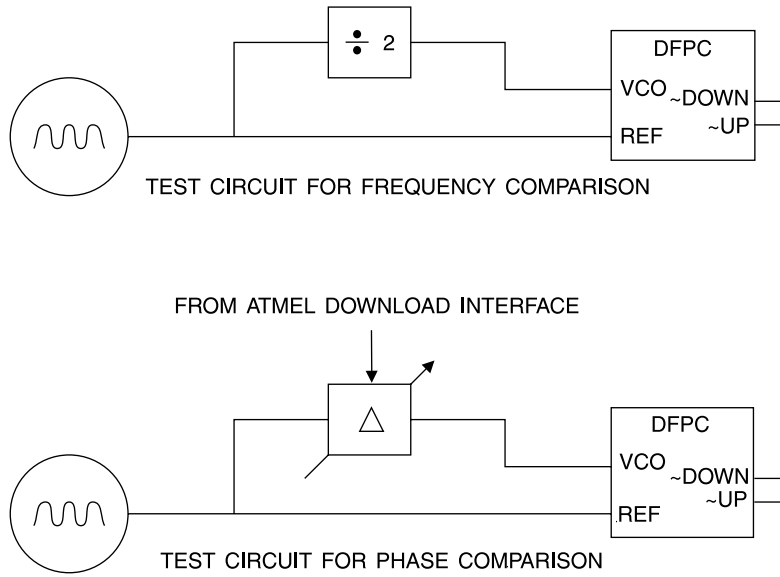


Figure 4. DFPC Timing Diagram

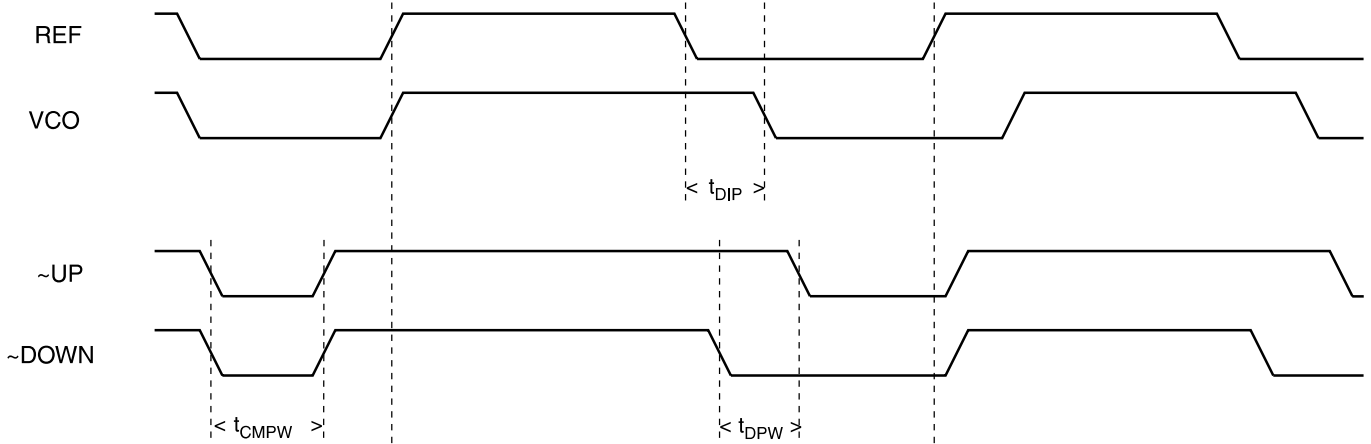


Table 1. 16 × 8 FIFO

	Cell Count ⁽¹⁾	Minimum Bounding Box (X × Y)	t _{CMPW} ⁽²⁾	t _{DPW} - t _{DIP} ⁽²⁾
DFPC	24	3 × 8	10.5 ns	0.5 ns

- Notes: 1. Includes cells used as wires.
 2. Typical Operating Conditions: 25°C, 5.0V, AT6000-4.



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