IEEE 1149.1-1990 Standard Test Access Port and Boundary Scan

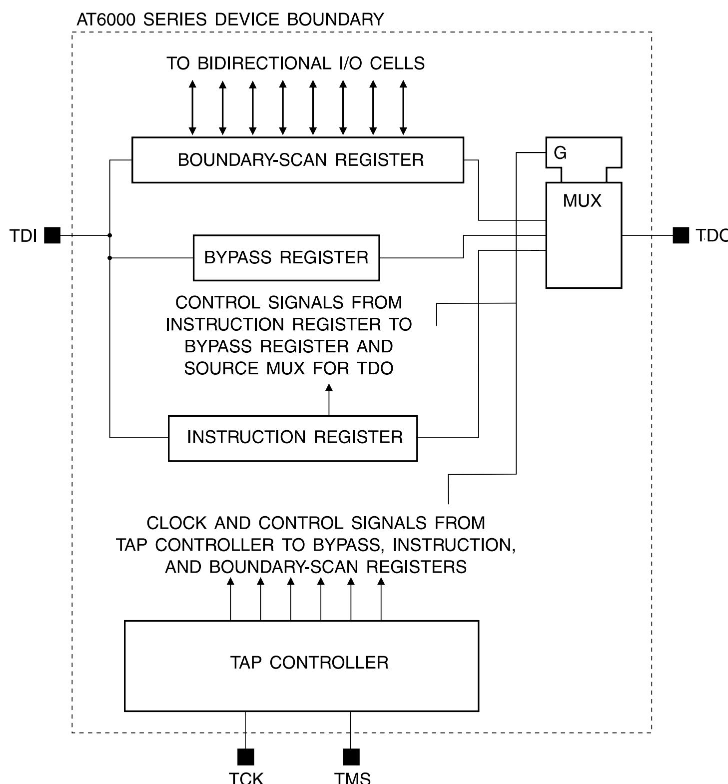
Field Programmable Gate Array

Application Note

Introduction

For system or board diagnostics, AT6000 Series devices can be programmed with the 1149.1 standard test logic and then reprogrammed for normal operation when the diagnostics are complete. The area and performance overhead of the test logic does not impact normal operation in the device because it is replaced by the logic for normal function. All mandatory test instructions can be executed with this portable test logic configuration, which guarantees conformance to the 1149.1 standard. The 1149.1 standard provides a consistent mechanism for confirming that each component in a system performs its required function. Since AT6000 devices are factory-tested with test patterns that exercise all the programmable features, integrity is insured without having to rely on standard test logic. Standard test logic is best suited for checking the interconnections between devices on the board. Boards are often multi-layer and double-sided, making traditional board test methods, like the bed-of-nails approach, expensive and impractical.

Figure 1. Block Diagram of 1149.1 Test Logic Architecture



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Recommended Test Procedure

Figure 1 shows the test logic architecture with dedicated I/O pins TCK, TMS, TDI, and TDO for the 1149.1 standard. TCK and TMS control the Test Access Port controller, a state machine that regulates the flow of serial test patterns and results from TDI to TDO. The boundary-scan register communicates with all usable I/O pins, which are configured as bi-directional drivers. The bypass register enables data to be moved more quickly through the device by bypassing the boundary-scan register. The instruction register holds the test instruction that activates either the boundary-scan or bypass register, and also helps control the MUX that supplies the source for TDO.

The recommended procedure for using 1149.1 Boundary Scan is to program the part with the test logic during a system diagnostics routine, then initiate boundary-scan testing for the system or board. When the test is done, reload the AT6000 device with system logic for normal operation. This test method eliminates the optional test capabilities defined in the standard. For example, using the SAMPLE/PRELOAD test instruction to capture the state of the I/O for online diagnostics during normal operation is not possible since the test logic is replaced with system logic.

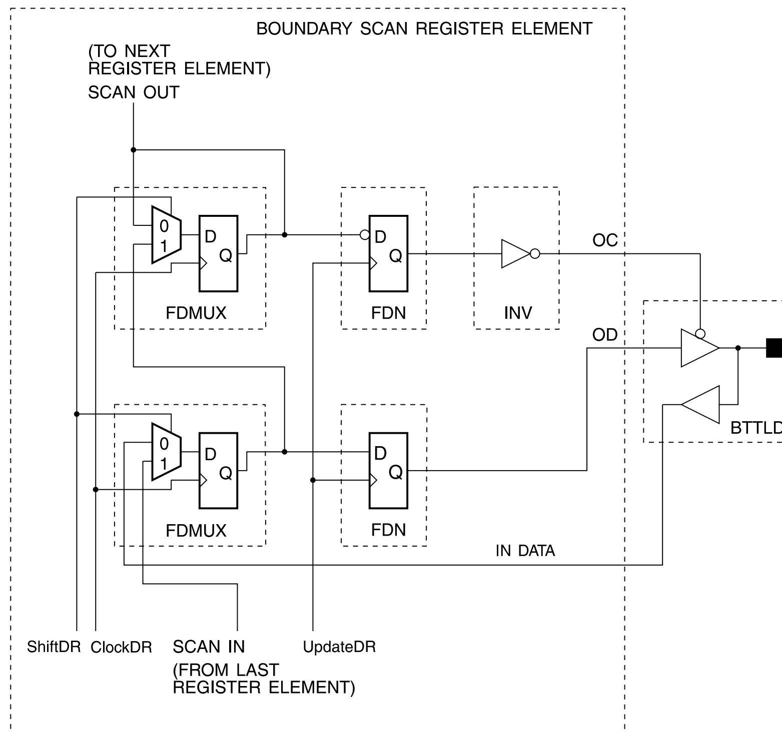
Other optional instructions facilitating internal fault testing and the execution of built-in self testing procedures (BIST) also cannot be supported with this test methodology.

For example, INTEST isolates the device, allows patterns to be serially shifted in and applied to the internal logic, then captures the output results within the device so that they can be shifted out for fault analysis. RUNBIST enables proprietary, built-in self-test procedures to be initiated by the standard test logic. The intended test capabilities of both these instructions are already covered by the factory testing performed on each AT6000 device. Therefore, eliminating these instructions and their associated overhead by loading and unloading the standard test logic does not increase the risk of overlooking a fault in the device.

Description of Boundary Scan Operation

As shown in Figure 2, the boundary-scan register element shifts data in through Scan In on the rising edge of ClockDR when ShiftDR is asserted. Since every I/O pin is configured as a bi-directional driver during the test sequence, two shift register bits are needed to control the output signal OD and the output control OC of the bi-directional driver. Each bit in the shift register is then latched to a secondary register that directly drives an output pin or output control of the bi-directional driver. UpdateDR loads the secondary registers from the shift register. If the bi-directional I/O BTTLD is set as an input (OC=1), the signal present at the pin is latched into the shift register on the rising edge of ClockDR when ShiftDR is unasserted.

Figure 2. Boundary Scan Cell



A mandatory 1149.1 requirement for programmable components is that the length of the boundary-scan register be independent of the way the component is programmed in normal system operation. Configuring every I/O to be bi-directional eliminates the dependency of the test logic on the particular I/O pin assignment utilized during normal operation. The test logic has the flexibility to set the direction of any I/O pin according to the patterns shifted in and transferred to the secondary registers that drive the output control pins. These patterns are formulated by the test engineer based on specific knowledge about the I/O pin assignment of the device during normal operation, and how the device is interconnected with other components on the board.

These secondary registers hold a pattern at the output pins while the results are sampled at the chip inputs and stored in the shift register. ShiftDR controls sampling and shifting of the data in the shift register. The secondary registers hold the output control pins stable during sampling and shifting out of the result for interpretation because the values in the shift register change. If the secondary registers were eliminated, then the shift-register element might incorrectly drive the output control during data shifting. More than one output from different devices might accidentally drive the same wire for a substantial period of time, which could damage the devices. Having a secondary register to hold the bi-directional output control signals during shifting prevents this.

Sampling and shifting is controlled by a synchronous state machine within the device. Control signals ClockDR, UpdateDR, and ShiftDR originate from this state machine, called a test-access-port (TAP) controller. External TAP signals – which might originate from automated test equipment (ATE) or a diagnostic processor – enter the capitalize controller through dedicated input pins and initiate state-to-state transitions. The following TAP signals go into the controller:

TCK: Test Clock input provides an independent clock signal for the test logic (i.e., boundary-scan register, instruction register, bypass register, and state machine).

TMS: Test Mode Select input controls the transitions of the TAP state machine, which determines when data is sampled, loaded, and shifted.

TDI: Test Data Input is the serial data input into the shift register for the test pattern.

TDO: Test Data Output is the serial data output from the shift register.

The signals TDI and TDO, although considered part of the TAP, do not initiate or affect the state-to-state transitions in the TAP controller. They provide the serial link to and from other components on the board. For a detailed state diagram of the TAP controller, refer to Chapter 5 of the JTAG (Joint Test Action Group) standard.

Composing a Test Pattern for the AT6005

The test pattern has two purposes: first, to set the I/O as either inputs to or outputs from the device, and second, to provide a logical value (“1” or “0”) to the output drivers from the device. The designer or test engineer is responsible for composing the pattern so that the proper inputs and outputs will be present on the device boundary. By performing the following tasks, any designer or test engineer somewhat familiar with the 1149.1 standard can prepare the patterns for boundary-scan testing:

1. Determine which pins are inputs and outputs based on how the AT6005 device is used in the board during normal system operation.
2. Compose a test pattern that will set the I/O to match the pin assignment according to the following assumptions:
   a. The AT6005 has 104 usable I/O because four dedicated I/O are needed for the TAP signals TCK, TMS, TDI, and TDO.
   b. Since a pair of bits are needed to set the direction of each of the 104 I/O, each pattern must be 208 bits in length.
   c. Since the pattern is loaded serially starting at TDI, the first bit-pair loaded sets the last I/O pins.
   d. For each pair of bits, the first serially loaded bit determines the I/O direction (input or output). A logical “1” sets the I/O as an input, a logical “0” sets the I/O as an output.
   e. For each pair of bits, the second serially loaded bit of the pair is relevant only if the first serially loaded bit of the pair was a “0”. The second bit can be either a “0” or a “1” and it will drive the output pin.
   f. Any unused pin should be driven to a high-impedance state by setting the first bit of its corresponding bit-pair to a “1” value.
   g. While the pattern is being loaded, the output pins are set to the high-impedance state until the secondary registers (see Figure 2) are updated with the test pattern value.
   h. The TAP signals TCK, TMS, TDI, and TDO use pins 131, 129, 132, and 128, respectively.

Figure 3 shows a test pattern in the boundary-scan register and its effect on the BTTLD bi-directional I/O. Pin 2 is set as an input because the output enable signal of BTTLD is set to “1.” Since the I/O is set as an input, the value of the first bit in the corresponding bit-pair in the boundary-scan register that drives the output buffer portion of BTTLD really does not matter (it is represented as an “X”). Pins 5 and 127 are also set as inputs because their output enable bits for BTTLD are also set as “1” in the boundary-scan register.

If the second bit of the bit-pair that controls the BTTLD I/O macros were a “0,” as is the case with Pins 3 and 126, the BTTLDs are set as outputs. The outputs of BTTLD for Pins 3 and 126 are both driven by the first bit of the corresponding bit-pair in the boundary-scan register. A “1” from the boundary-scan register drives Pin 3, and a “0” drives Pin 126.

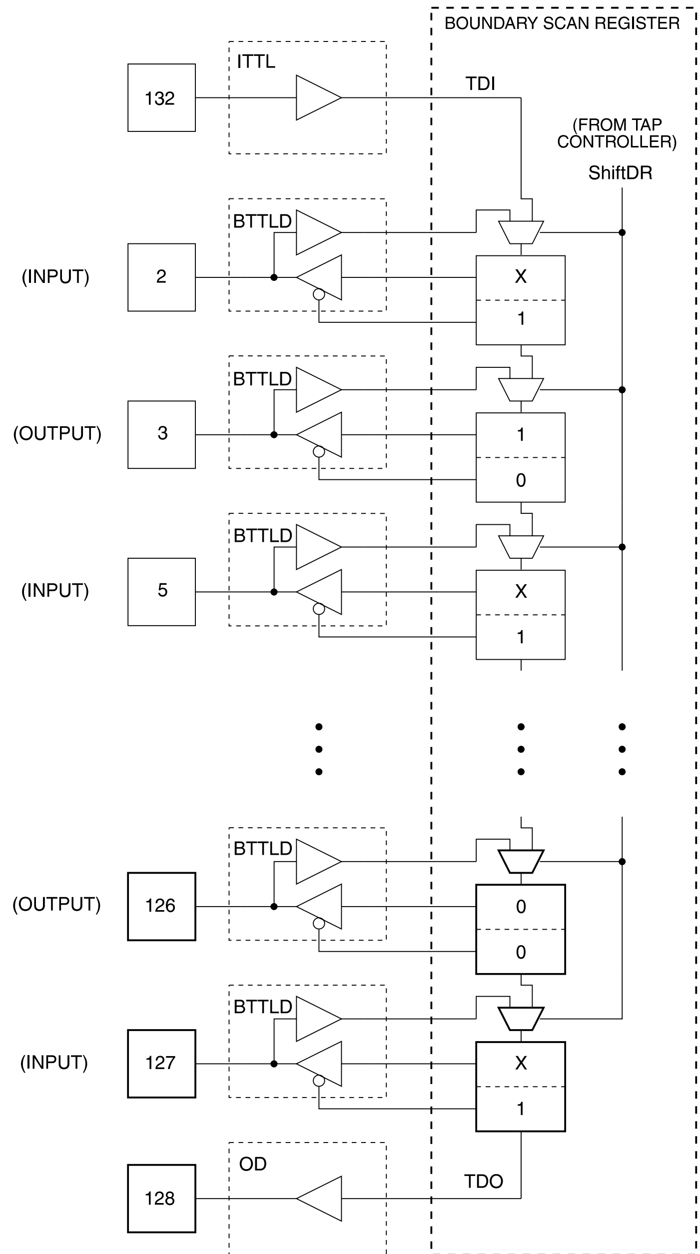
A test pattern is serially shifted in through Pin 132. For example, the first bit-pair is shifted through the entire boundary-scan register until it is in position to set the BTTLD macro of pin 127. While the pattern is being shifted through the register, the outputs of the secondary registers that the drive the output enable pins of the BTTLD macros are set to “1” so that every I/O in the device is in the high-impedance state (see Figure 2). This precautionary measure prevents device pins from driving a signal onto a board wire that might contend with a signal from another chip. When the pattern is completely shifted into the boundary-scan register, the secondary registers are updated with the pattern, thus setting the direction of the BTTLD macros.

Test Logic Architecture

Figure 4 shows a more detailed schematic of the test logic. The TAP controller performs boundary-scan by first capturing signals at the input pins of the bi-directional drivers and loading them into a corresponding shift register element. The TAP controller sets ShiftDR low and takes ClockDR from low to high to perform the capture. The captured input signals originate from the outputs of other chips on the board as the result of a previous test pattern. Shifting the captured pattern out of the device occurs when the TAP controller sets ShiftDR high and toggles ClockDR. While the result is being shifted out through TDO, a new test pattern is simultaneously being shifted in through TDI. The new pattern is loaded into the secondary registers when the TAP controller toggles UpdateDR. Any bi-directional driver that is set as an output will then drive the board wires leading to the inputs of other chips.

Also shown in Figure 4 are bypass and instruction registers. The bypass register quickly passes test patterns through the device if the patterns are designated for another component on the board. Captured test pattern results also flow through the bypass register to hasten their arrival to another part of the diagnostics system. Depending on the instruction loaded into the instruction register, either the bypass register or the boundary-scan register provides the source for TDO. The logical value loaded into the instruction register controls the multiplexer MUX that selects either the boundary-scan or bypass register to drive TDO.

Figure 3. Test Pattern in Boundary-Scan Register



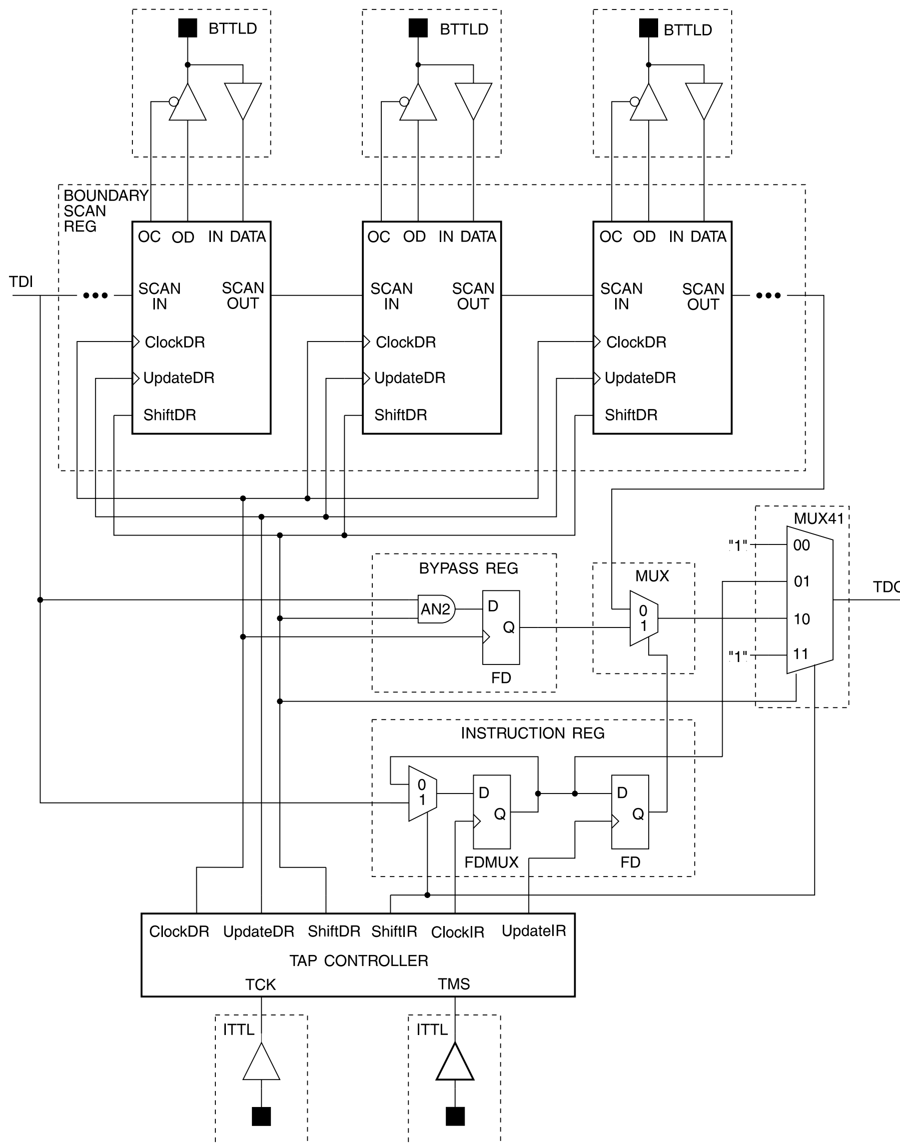
The following mandatory instructions are necessary to conform to the standard (as described in Chapter 7 of the JTAG standard):

BYPASS: Causes a serial test pattern being shifted into TDI to be passed through a single bit register (called the bypass register) and then to TDO. The purpose of this instruction is to allow rapid serial movement of test patterns and results between components on a board. The instruction register should be load with a logical "1" value to initiate BYPASS.

SAMPLE/PRELOAD: Allows a snapshot of the data present at the input pins of a device to be stored in the shift register, and then allows the snapshot to be shifted out through TDO. While the data is being shifted out, a new test pattern can be simultaneously shifted in through TDI. The instruction register should be load with a logical "0" value to initiate SAMPLE/PRELOAD.

EXTEST: Allows the test pattern held in the shift register to be loaded into secondary registers that drive the output pins of the device. The application of this instruction lets the outputs of a device to drive the board traces so that the inputs of other devices can take a snapshot of the values on those traces, and thus determine if the board traces were manufactured properly. The instruction register should be loaded with a logical "0" value to initiate EXTEST.

Figure 4. Schematic of 1149.1 Test Logic Architecture



The TAP controller loads the instruction register the same way it loads the boundary-scan register. A functionally analogous but independent set of signals, ClockIR, UpdateIR, and ShiftIR are used to control loading and shifting in the instruction register. Changing the level of TMS before the rising edge of TCK initiates state-to-state transitions in the TAP controller for every TCK cycle, causing the outputs of the controller (ClockDR, ShiftDR...) to change. A particular sequence of level changes in TMS over several TCK cycles results in the execution of either SAMPLE/PRELOAD or EXTEST if the value in the instructions register is a logical “0.”

The TAP controller also chooses the register (boundary-scan, bypass, or instruction) that drives TDO. When the ShiftDR signal is asserted either the boundary-scan register or the bypass register is selected. The instruction register must then determine the register to drive TDO. If the instruction register is loaded with a “1,” meaning that the BYPASS instruction should be executed, then the bypass register is selected. A logical “0” in the instruction register means that either the EXTEST or SAMPLE/PRELOAD should be executed, and that the boundary-scan register is selected.

When the ShiftIR signal is asserted the instruction register is selected to drive TDO regardless of the current instruction. If both ShiftIR and ShiftDR are unasserted, then driving a logical “1” through the multiplexer deactivates TDO.

Operating Conditions

The minimum recommended cycle time for TCK is 100 ns (10 MHz) for correct operation. With careful floor planning of critical path control signals, TAP controller the performance could be improved to 15 MHz. In the AT6005, at a TCK speed of 10 MHz, two bits are needed for each of the 104 bi-directional I/O. Shifting in a new test pattern takes 20 µs. When the boundary-scan test is complete, the device is reconfigured for normal operation in 6.4 ms by serially loading the stream of bits into the SRAM that programs the logic and interconnections. The device can be reconfigured in 808 µs if the bit stream is loaded as 8 bit bytes. A complete 1149.1 circuit is available in schematic and layout form.

References

IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std. 1149.1-1990, Joint Test Action Group (JTAG), Institute of Electrical and Electronic Engineers (IEEE), New York, Mary 21, 1990.

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