



16-word by 8-bit FIFO

Introduction

The AT6000 Series field programmable gate array (FPGA) lets the designer implement a synchronous first-in, first-out (FIFO) register buffer with a word width and depth tailored to specific design needs. A 16-word FIFO with each word being eight bits is constructed and analyzed in the AT6005-2 device, and shown to have 15 MHz performance.

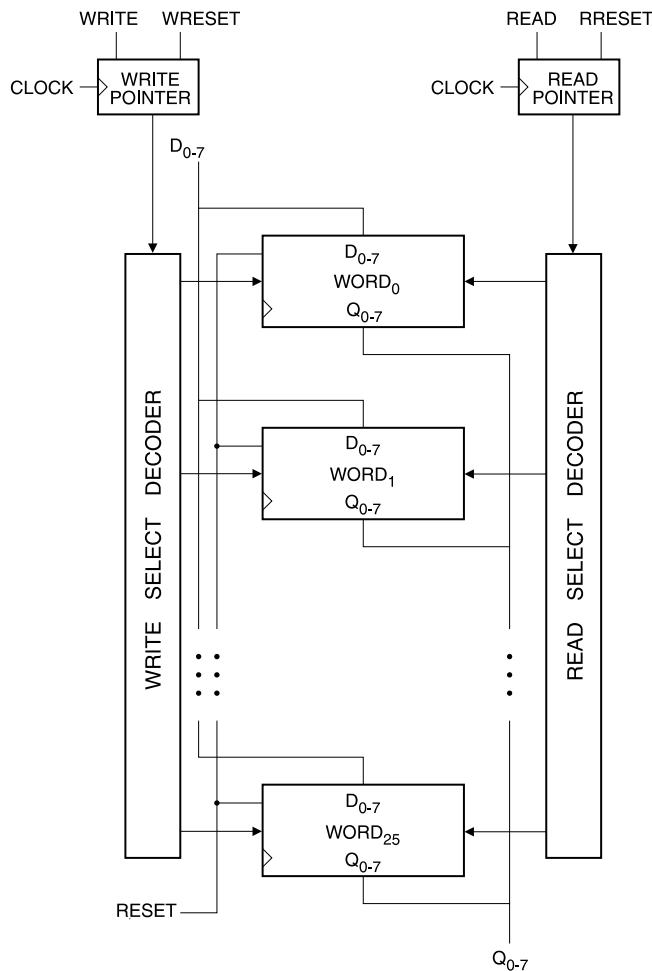
Description

Figure 1 shows a functional block diagram of the FIFO architecture. Data on inputs D_{0-7} is latched into a particular word register on the rising edge of CLOCK when WRITE is asserted. When READ is asserted, the outputs Q_{0-7} are driven by a new word register. The write and read pointers, together with the select decoder logic, determine the particular register or registers that are the

Field Programmable Gate Array

Application Note

Figure 1. Architecture of 16×8 FIFO



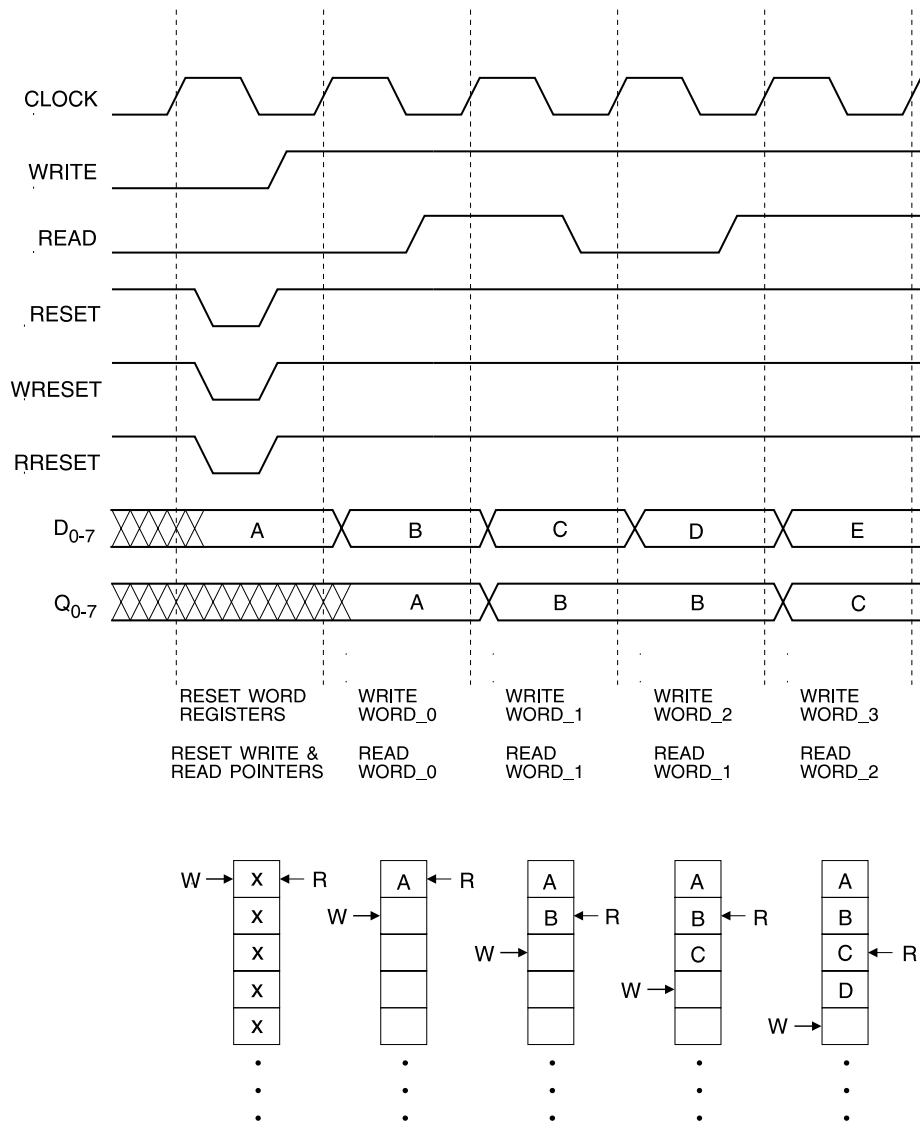
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target of the write operation and the source of the read operation. Individual read or write operations can be executed every clock cycle when either the READ or WRITE signals are asserted. Simultaneous write and read operations are also possible to any one word register or combination of two registers. If neither the READ or WRITE signals are asserted, the pointers maintain their current address. After a write operation occurs, the write pointer is automatically updated to point to the next word register, and then awaits the next write operation. The read pointer allows the data of a particular word register to be continuously available until the next read operation, after which new data from the next word register is accessed. Essentially, the read pointer points to the last word that was read and the write pointer points to the next word to be written.

The RESET, WRESET, and RRESET signals control the initialization of various portions of the FIFO. When RESET is set low, the word registers are immediately cleared. RESET is an asynchronous signal that causes all bits within each word register to be set low. WRESET and RRESET are synchronous initialization signals for the write and read pointers. If WRESET is taken low and then high before the rising edge of CLOCK, the write pointer is set to the first word register. A write operation can then commence on the next rising edge of CLOCK if WRITE is asserted. The RRESET signal controls the read pointer in the exact same manner. Figure 2 shows the operation of the FIFO from the relative timing of the control signals.

Figure 2. Relative Timing of FIFO Control Signals



A schematic of the word registers is shown in Figure 3. Each bit of the data word is stored in an FDMUX macro, which is a two-to-one multiplexer feeding a D-type flip-flop. If the word register is selected for a write operation, the two-to-one multiplexer chooses D_{0-7} as the input to be latched into the D-type flip-flop on the next rising edge of CLOCK. If the word register is not chosen for a write operation, the two-to-one multiplexer recirculates the data value already present in the D-type flip-flop. When a READ operation is initiated, the logic values present at the D-type flip-flop outputs are passed through the tri-state output buffers BUFZ onto an internal tri-state bus that ties together the output of every word register. Since the inputs D_{0-7} and outputs Q_{0-7} enter and exit on different wires, simultaneous write and read operation can occur on the same clock cycle.

Incorporated into each word register is a portion of the read and write pointer logic. The write pointer is a controlled shift register that is 16 bits in length. Upon initialization the first bit in the shift register is set to a logical "one" value, and all other bits are reset low. After a write operation occurs to the first word register, the "one" is passed to the next bit in the write pointer shift register at the rising edge of CLOCK.

This "one" bit will continue to loop around the shift register whenever WRITE is asserted upon the rising edge of CLOCK. As the "one" is passed along, it allows a write operation to occur to the word register. The read pointer is implemented in essentially the same manner.

In the AT6000 architecture, implementing the write and read pointers as controlled shift registers has several advantages over controlled counter/decoder methods. For example, several 5-bit modular 16 counters together with several 5-bit to 16-bit decoders could be used to implement the read and write pointers in a controlled counter/decoder approach. Although the counters would use far less flip-flops, the decoder logic would be five times as large as in the controlled shift register method. More control signals would also have to be bused to every word register since in the controlled counter/decoder method every output bit of the counters must be used as a select control for the decoders of both the read and write pointers. The additional decoder logic and busing necessary for the controlled counter/decoder makes it ostentatiously large. Since every cell in the AT6000 architecture contains a D-type flip-flop, the controlled shift register approach is more efficient than the controlled counter/decoder approach.

Figure 3. Modular Word Register Schematic

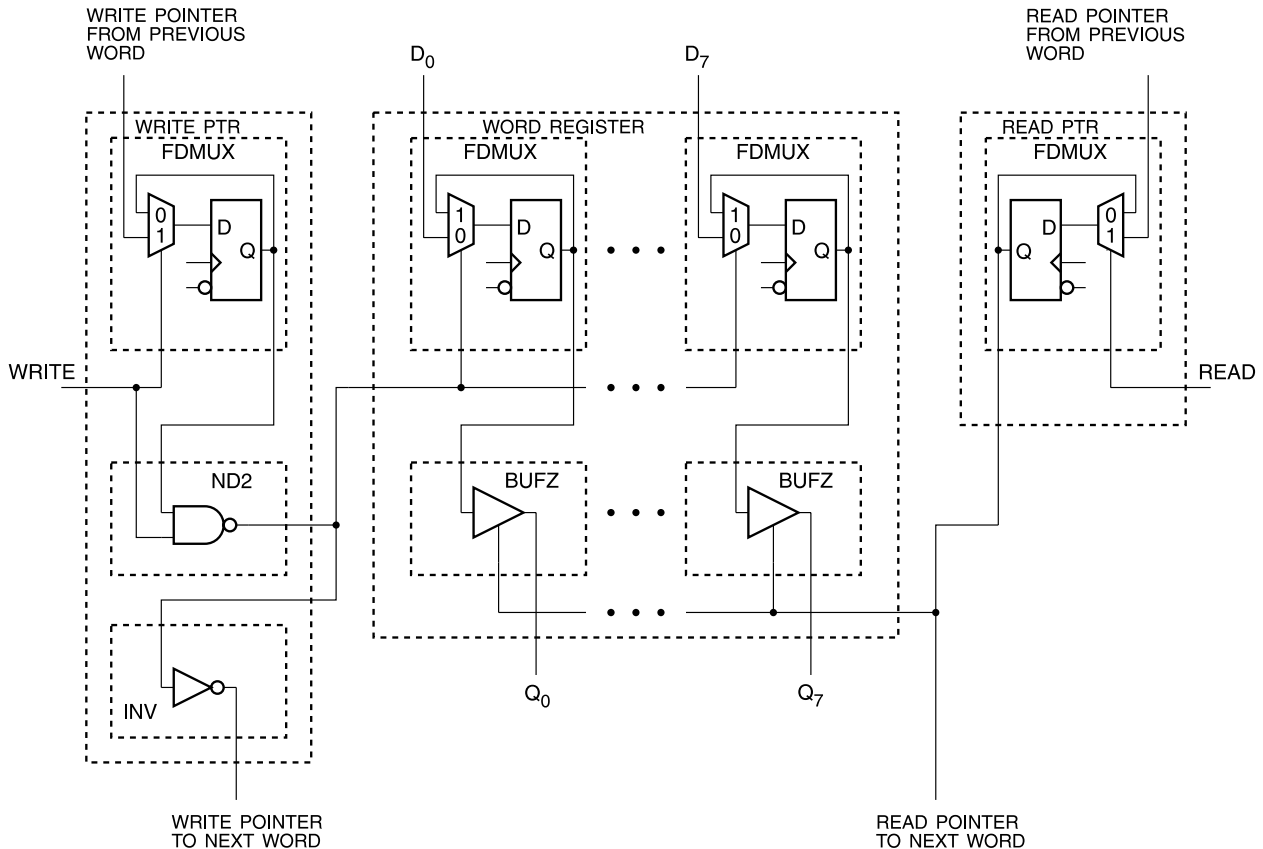


Figure 4 shows the initialization logic along with several word registers. The initialization logic synchronously allows either the write or read pointers to be individually or simultaneously reset to point to the first word register. The word registers can be asynchronously cleared. For this example, 16-word registers are linked together to form a 16-word FIFO, with each word being eight bits in length. The modular construction allows the concatenation of word registers to form a FIFO of any length. The word registers can also

be widened as long as the portions of the write and read pointers are maintained on either side. Only one unique register is needed to hold the initialization logic to mark the first word of the FIFO.

The performance and utilization statistics for the 16-word by 8-bit FIFO are given in Table 1. This implementation is available in schematic and layout form.

Figure 4. Architecture of 16-word x 8-bit FIFO

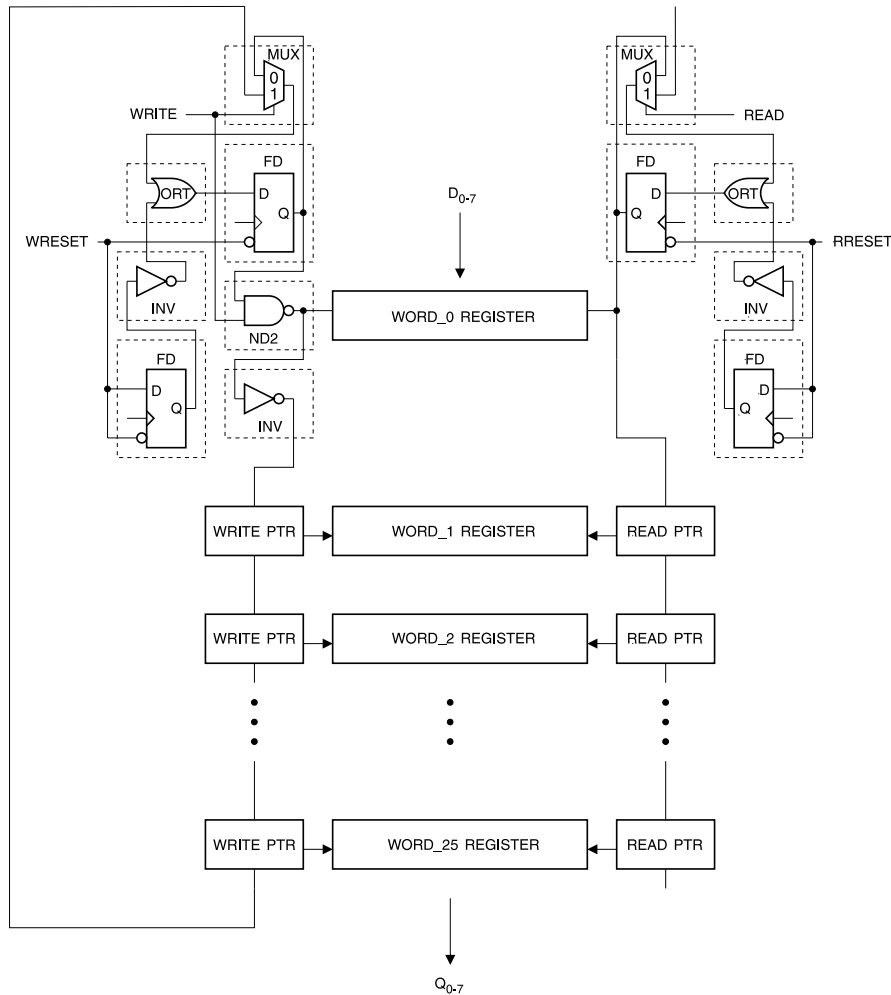


Table 1. 16 x 8 FIFO

FIFO	Cell Count ⁽¹⁾	Minimum Bounding Box (X × Y)	Cells Per Bit-4 ⁽²⁾	Maximum Speed ⁽³⁾
16-word by 8-bit	653	20 × 35	5	66.7 ns/15 MHz

- Notes:
1. Includes cells used as wires.
 2. Amortizes the quantity of cells used for write and read pointers in each 8-bit word register over the cell count for each bit of the register. A 16-bit word register would use 4.5 cells per bit.
 3. READ → Q₀₋₇. Worst-case Commercial Operating Conditions: CLK → C₀, 70°C, 4.75V.



Atmel Headquarters

Corporate Headquarters

2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe

Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia

Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan

Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs

1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset

Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand

North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

BBS

1-(408) 436-4309

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