



## 8-bit, S-P/P-S “Corner-Bender” Data Converter

### Introduction

With the proliferation of computer and voice networks that carry digitized analog data, data conversion applications have become commonplace. For example, the use of time-division multiplexing in broadcasting and receiving circuitry requires fast serial-to-parallel (S-P) and parallel-to-serial (P-S) data conversion. Using the AT6005 device, two S-P/P-S corner-bender circuits were implemented: one optimized for area and power consumption, the other for speed and expandability.

### Description

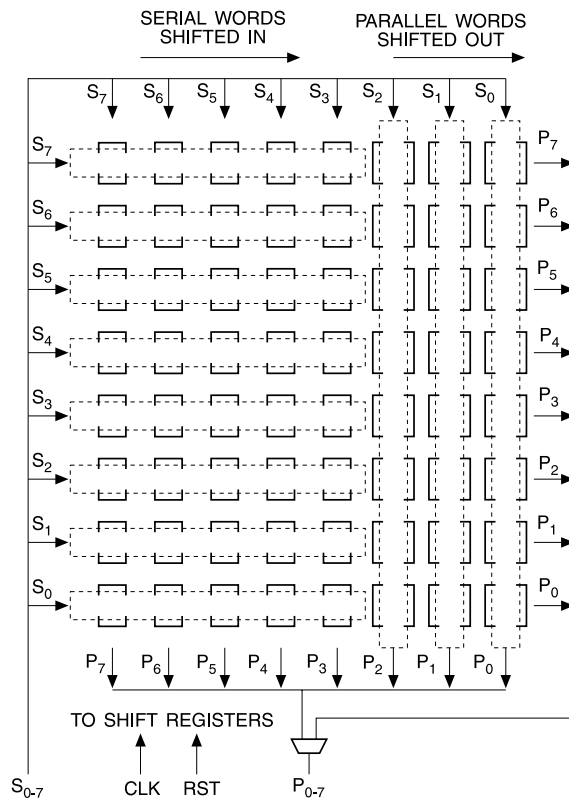
Figure 1 is the functional representation for an 8-bit corner-bender. CLK is the clock input signal and RST is the asynchronous reset. RST is active low. Pins  $S_0$  through  $S_7$  are the data inputs; pins  $P_0$  through  $P_7$  are the converted data outputs.

The corner-bender accepts 8-by-8 blocks as input. Each block is eight bits wide and arrives serially over eight clock cycles. The corner-bender transforms each input block into an 8-by-8 output block such that bits aligned in parallel in the input block are aligned serially in the output block, and vice versa.

## Field Programmable Gate Array

## Application Note

Figure 1. Functional Representation of Corner-bender



Rev. 0472C-09/99



The two implementations – low-area/low-power and high-speed/expandable – are functionally identical. Initial power-up of the AT6005 device resets all user registers, so the circuit begins data conversion on the first rising edge of CLK after configuration.

In serial-to-parallel mode, the  $P_{0-7}$  outputs remain low for the first seven clock cycles. After the rising edge of the eighth clock cycle, the first 8-bit serial data word from  $S_0$  is available at the  $P_{0-7}$  outputs. The  $S_1$  serial word is available after the rising edge of the next clock (Figure 2). Subsequent serial words are available on the rising edge of every clock until RST is asserted. Asserting RST at any time clears the registers and inhibits the conversion.

The first implementation minimizes area and power consumption, but still operates at up to 22 MHz in the AT6005-4 and 31 MHz in the AT6005-2.

Figure 3 shows the gate-level equivalent of the register block structure used for conversion. A single AT6005 cell is configured as a two-input multiplexer feeding a D-type flip-flop (FDMUX).

After the rising edge of every eighth clock cycle, two-to-one multiplexers switch the direction of the data flow into the register from west-to-east to north-to-south. The boundary registers that feed the outputs,  $P_{0-7}$ , are also switched after the rising edge of every eighth clock cycle. Pins  $P_{0-7}$  receive parallel (or serial) data from the boundary registers on the axis perpendicular to, and on the opposite side of, the serial (or parallel) data input.

The second implementation maximizes throughput and can operate at 52 MHz (AT6005-4) and 75 MHz (AT6005-2),

but requires almost twice the area and 25 percent more power per MHz than the first.

A secondary set of registers is used to latch a parallel (or serial) 8-bit word from a serial (or parallel) data register on the rising edge of every eighth clock cycle. Figure 4 shows the gate-level equivalent of the register block structure used for the conversion. The shift registers employ D-type flip-flops (FD); the secondary registers use FDMUX macros.

At the rising edge of every eighth clock cycle, the secondary registers load a parallel (or serial) 8-bit data word from the serial (or parallel) shift registers. On subsequent clock cycles, the parallel (or serial) words are shifted from each set of secondary registers until the words reach  $P_{0-7}$ .

The slower implementation requires fewer cells and uses less area, but has a longer critical path delay and hence less throughput than the faster implementation. In the first implementation, the longest interconnection occurs between the registers containing the most significant bit,  $S_0$ , which feeds the two-to-one multiplexer driving  $P_7$ , MUX21 (Figure 5).

The longest path between the register and multiplexer spans nearly half the circumference of the layout, which is four times longer than the longest path in the second implementation. Each flip-flop in the second circuit connects to only its two nearest neighbors, making the interconnects fairly equal in length. As a result, the second implementation can be expanded without significant performance loss. Table 1 gives a comparison of the performance and utilization statistics for the two corner-benders. Both circuits are available in schematic and layout form.

**Figure 2.** Timing Diagram of Serial-to-Parallel Corner-bender Operation

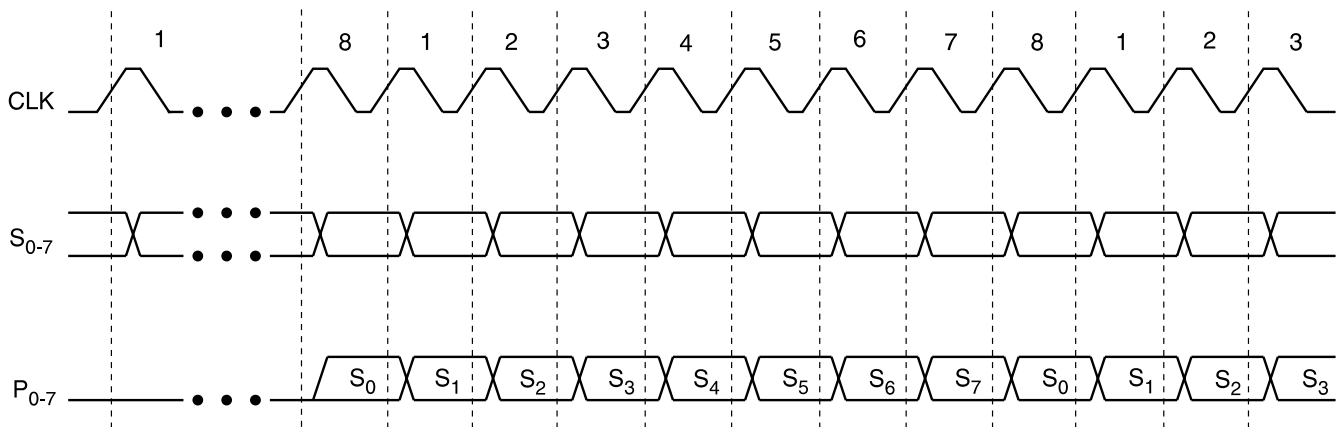


Figure 3. Schematic of Low-area/Low-power Core

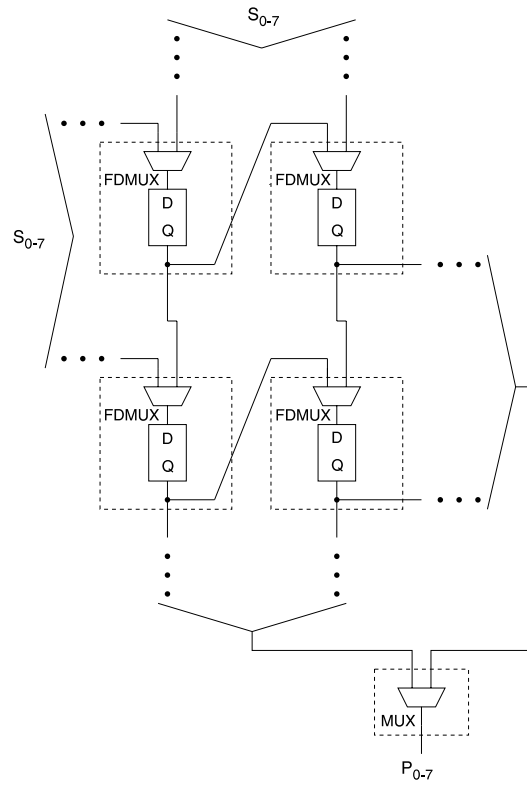
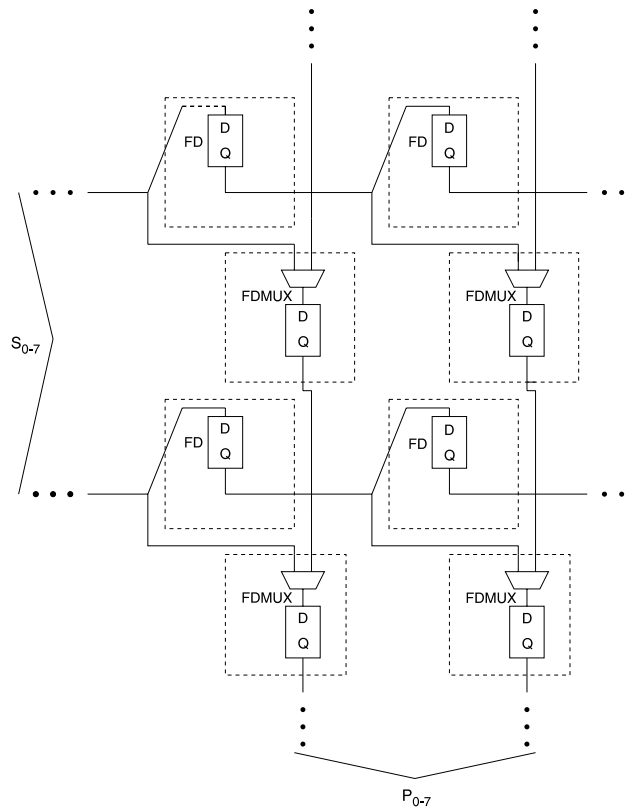
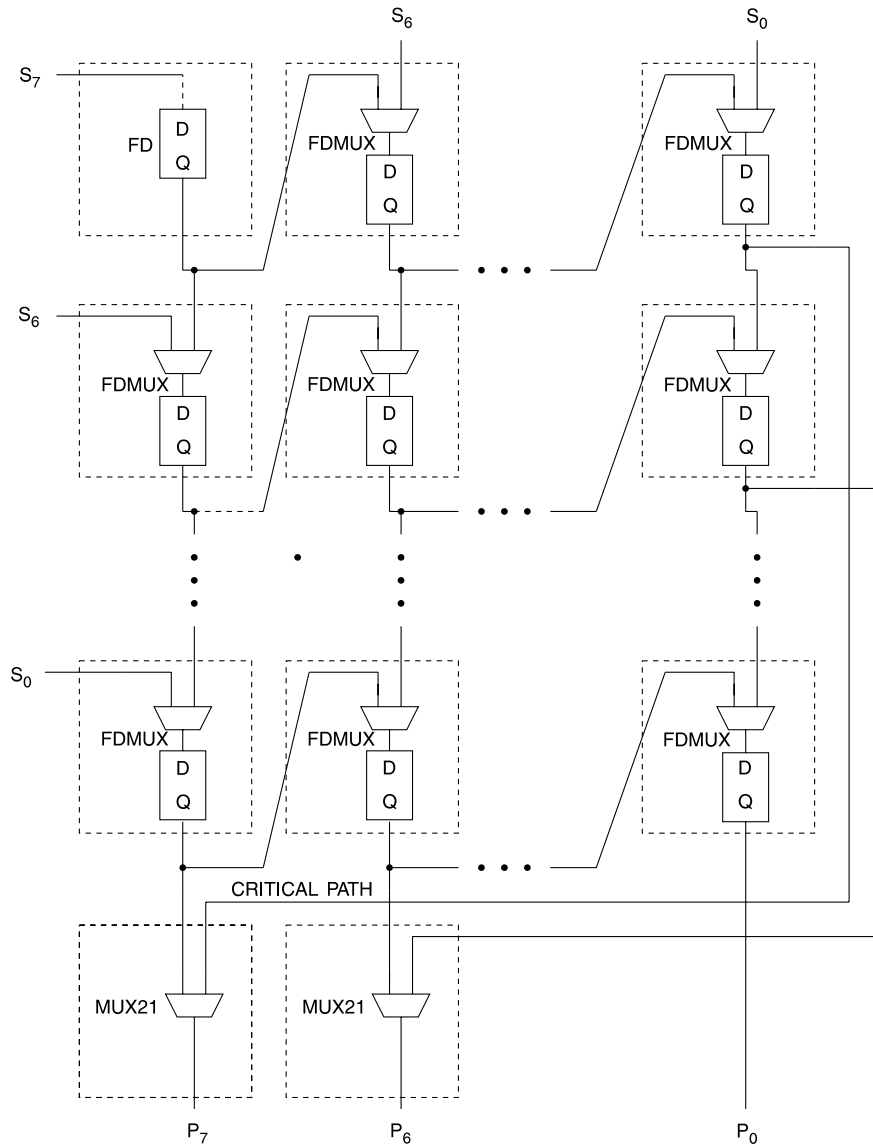


Figure 4. Schematic of High-speed/Expandable Core



**Figure 5. Interconnect Scheme of First Implementation**



**Table 1. Statistics for Corner-benders**

Corner Bender	Cell Count <sup>(1)</sup>	Minimum Bounding Box (X × Y)	Maximum Speed AT6005-4 <sup>(2)</sup>	Maximum Speed AT6005-2 <sup>(2)</sup>
Low Area/Low Power	164	16 × 12	45.5 ns/22 MHz	32.3 ns/31 MHz
High-speed/Expandable	260	15 × 19	19.2 ns/52 MHz	13.3 ns/75 MHz

Notes: 1. Includes cells used as wires.  
 2. CLK → P<sub>0</sub>. Worst-case Commercial Operating Conditions: 70°C, 4.75V.



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