16-bit Four-to-One Multiplexer with 15 ns Delay

Field Programmable Gate Array

Application Note

Introduction

The AT6000 Series field programmable gate array (FPGA) lets the designer implement a 16-bit, four-to-one multiplexer with a 15 ns delay from the select control to the most significant output bit. Performance is enhanced by a unique feature of the busing architecture that enables the select control lines to be distributed across the multiplexer data path with minimal skew.

Description

Figures 1 and 2 show the relative physical placement of the logical cells that compose the multiplexer function and the busing structure that performs the interconnection. Four 16-bit input buses, A_{0-15}, B_{0-15}, C_{0-15}, and D_{0-15}, can be multiplexed to a 16-bit output bus F_{0-15}. Two select lines S_0 and S_1 determine which of the input buses are multiplexed to the output. Figure 1 shows several four-to-one multiplexer bits, each implemented in four cells. A cell can be configured as a two-to-one multiplexer (MUX21). Every MUX21 is tied to either the S_0 or S_1 select lines. S_0 controls 32 MUX21 cells, and S_1 controls 16 MUX21 cells.

Typically, distribution of a signal to such a large number of cells would cause unacceptable skew between the cells closest and furthest from the source. By aligning the multiplexers, and routing a single wire to every one, the most efficient signal distribution method is realized. However, the load on the wire might unacceptably decrease its slew rate. Buffering the wire after routing it to a certain number of multiplexers would improve the slew rate, but additional cells would be required for the buffering. Skew would also be introduced as buffer stages are added to the distribution network. Other signal distribution methods have been shown to have minimal skew and optimal slew rate, but they require more logic resources.

Using express buses, skew is minimized and slew is improved by segmenting the load along each signal. Figure 2 shows that the express and local buses can distribute S_0 and S_1 without using additional logic cells. S_0 passes from a local bus into a repeater – a programmable crossbar buffer – and is routed onto the express bus. At each repeater stage, taps are taken off onto the local bus and into the multiplexers. Since the express bus is essentially an unloaded wire, its delay is much less than that of the local bus, which is loaded by multiplexer select inputs. Although signal propagation of S_0 and S_1 is serialized from the source output through several repeater stages to the final inputs, this distribution method is the most efficient for performance and cell utilization.

Table 1 gives performance and utilization statistics for the multiplexer. It is available in schematic and layout form.

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Figure 1. Schematic of Multiplex Function for Several Output Bits

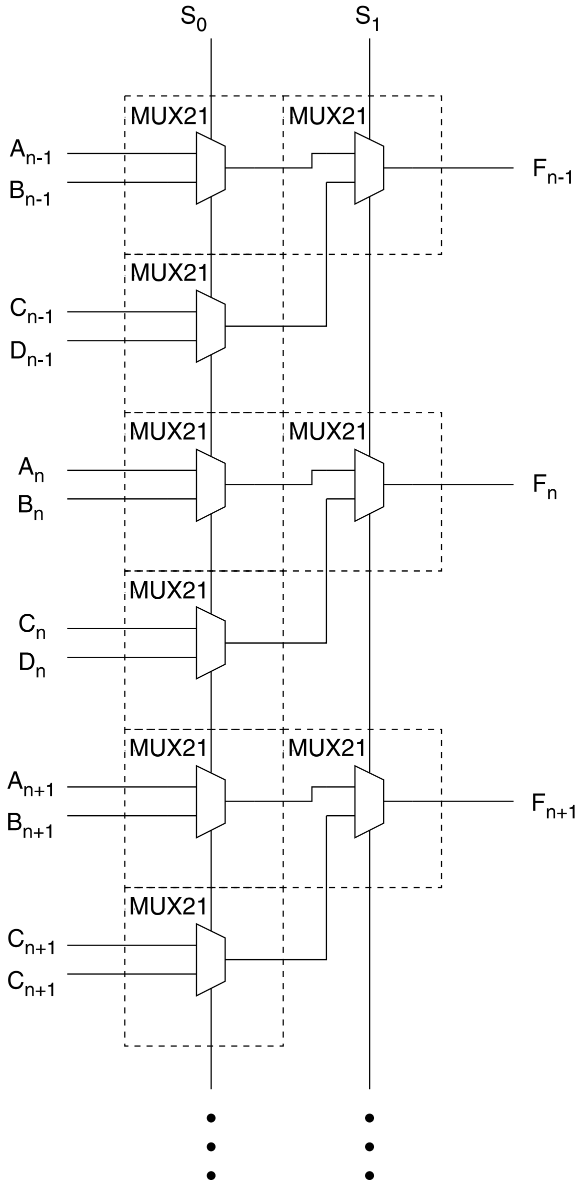

Figure 2. Equivalent Layout with Busing Structure

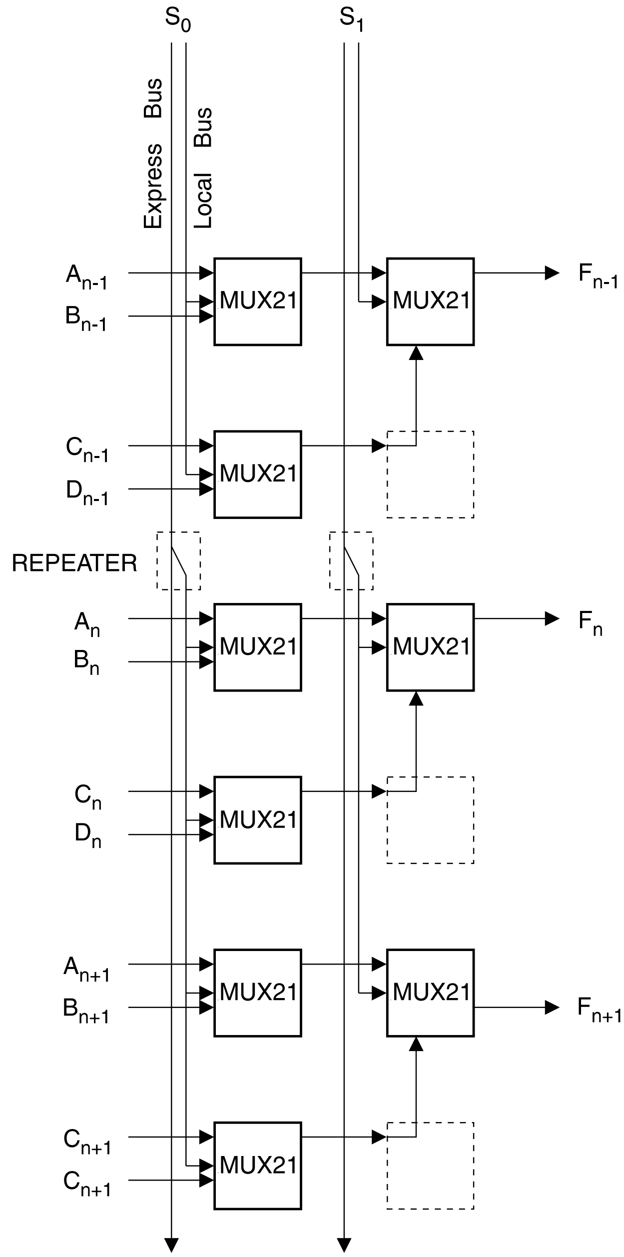

Table 1. Statistics for Four-to-One Multiplexer

Multiplexer	Cell Count[1]	Minimum Bounding Box ($X \times Y$)	Maximum Delay[2]
16-bit	64	2×32	15 ns/66.7 MHz

Notes: 1. Includes cells used as wires.
2. $S_0 \rightarrow F_{15}$. Worst-case Commercial Operating Conditions: 70°C, 4.75V.

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