



## 24-bit Magnitude Comparator with 50 ns Response

### Introduction

The AT6000 Series field programmable gate array (FPGA) lets the designer implement a magnitude comparator that can compare two 24-bit binary integers in 50 ns.

### Description

Figure 1 shows the structure of the magnitude comparator. Given two numbers  $A_{0-23} > B_{0-23}$ , the output GT will become asserted. If  $A_{0-23}$  is less than or equal to  $B_{0-23}$ , GT remains unasserted.

The logic necessary to compare two numbers can be derived iteratively

according to four equations. The first two determine the largest number:

$$1. T_n = A_n B_n'$$

For  $n = 0$ , where  $n$  is the significant bit.

$$2. T_n = A_n B_n' + T_{n-1}(A_n + B_n')$$

For  $n = 1$  to 23, where  $n$  is the significant bit.

The second two determine if the numbers are equal:

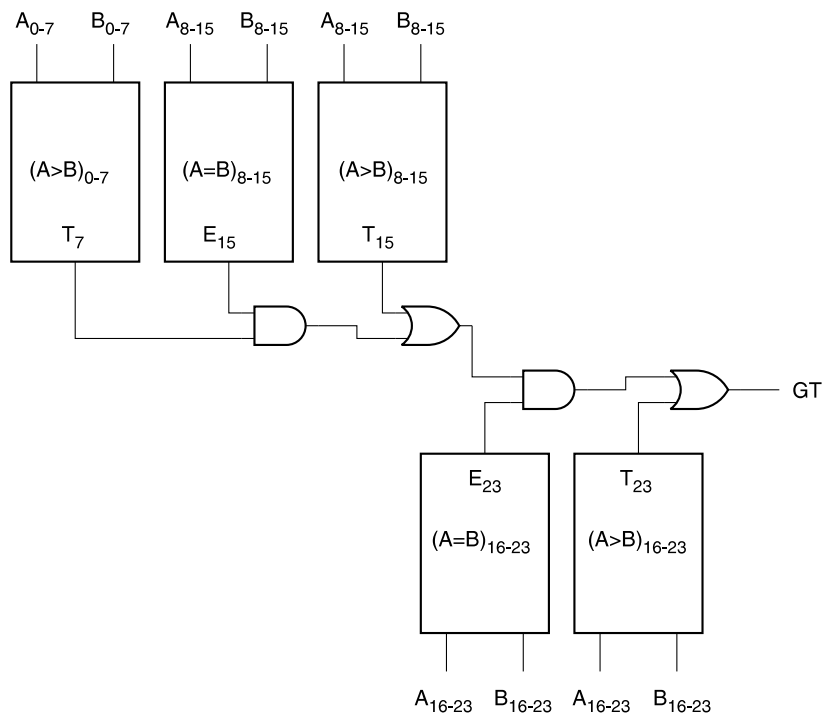
$$3. E_n = A_n' B_n + A_n B_n'$$

For  $n = 0$ , where  $n$  is the significant bit.

$$4. E_n = (A_n' B_n + A_n B_n') + E_{n-1}$$

For  $n = 1$  to 23, where  $n$  is the significant bit.

Figure 1. Structure of 24-bit Magnitude Comparator



## Field Programmable Gate Array

## Application Note



Equation  $T_n$  could be used exclusively to generate the logic for GT, but the circuit would have a delay equivalent to 48 two-input NAND (ND2) gates for the worst-case comparison conditions.

To improve performance, the comparator is partitioned into three stages that each compare 8-bit portions of the two numbers. Thus, the parallel comparison of the three 8-bit portions of both numbers is faster than a single 24-bit implementation. The delay through an 8-bit stage is equivalent to 16 two-input NAND (ND2) gates.

Within each stage, the circuitry performs a bit-wise comparison starting between the most significant  $A_n$  and  $B_n$  bits within each stage, and asserts stage  $T_{(m+1)(N/3)-1}$  (where stage  $m$  is 0 through 2, and  $N = 24$  the bit-width of the compared numbers), if the most significant  $A_n$  is asserted and  $B_n$  is unasserted ( $A_n > B_n$ ). If the most significant  $A_n$  and  $B_n$  bits are equal, then a pair of lesser significant bits within the

stage must determine if the magnitude of the aggregate quantity of A bits is greater than the B bits in stage  $m$ . Also, the circuitry within each stage performs a bit-wise comparison on each pair of bits and asserts  $E_{(m+1)(N/3)-1}$  if the 8-bit portions are equivalent.

The  $T_{(m+1)(N/3)-1}$  and  $E_{(m+1)(N/3)-1}$  outputs from each 8-bit stage are fed into some logic to derive GT. This logic can be determined according to the equation:

$$1. S_m = T_{(m+1)(N/3)-1}$$

Where  $m = 0$  is the significant stage and  $N = 24$  the total number of bits.

$$2. S_m = T_{(m+1)(N/3)-1} + E_{(m+1)(N/3)-1}S_{m-1}$$

For  $m = 1$  to 2, where  $m = 0$  is the significant stage and  $N = 24$  the total number of bits.

The final result S2 is equivalent to GT.

**Figure 2.** Implementation of Magnitude Comparator

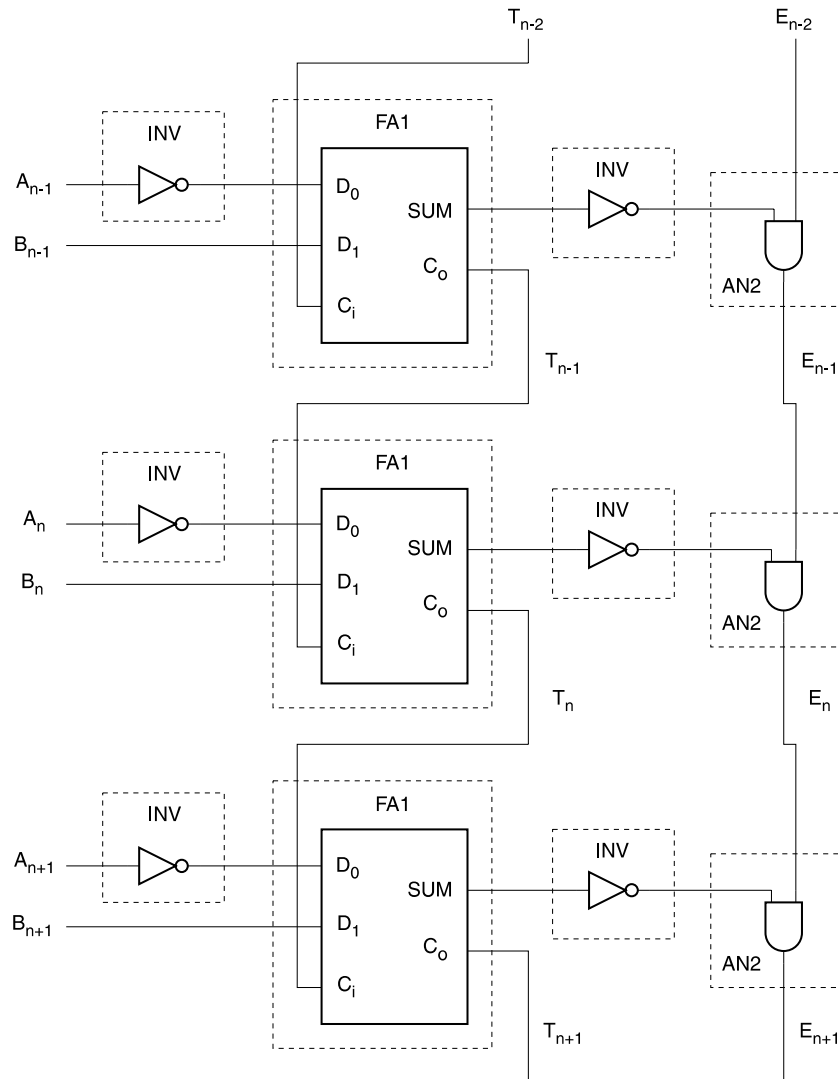
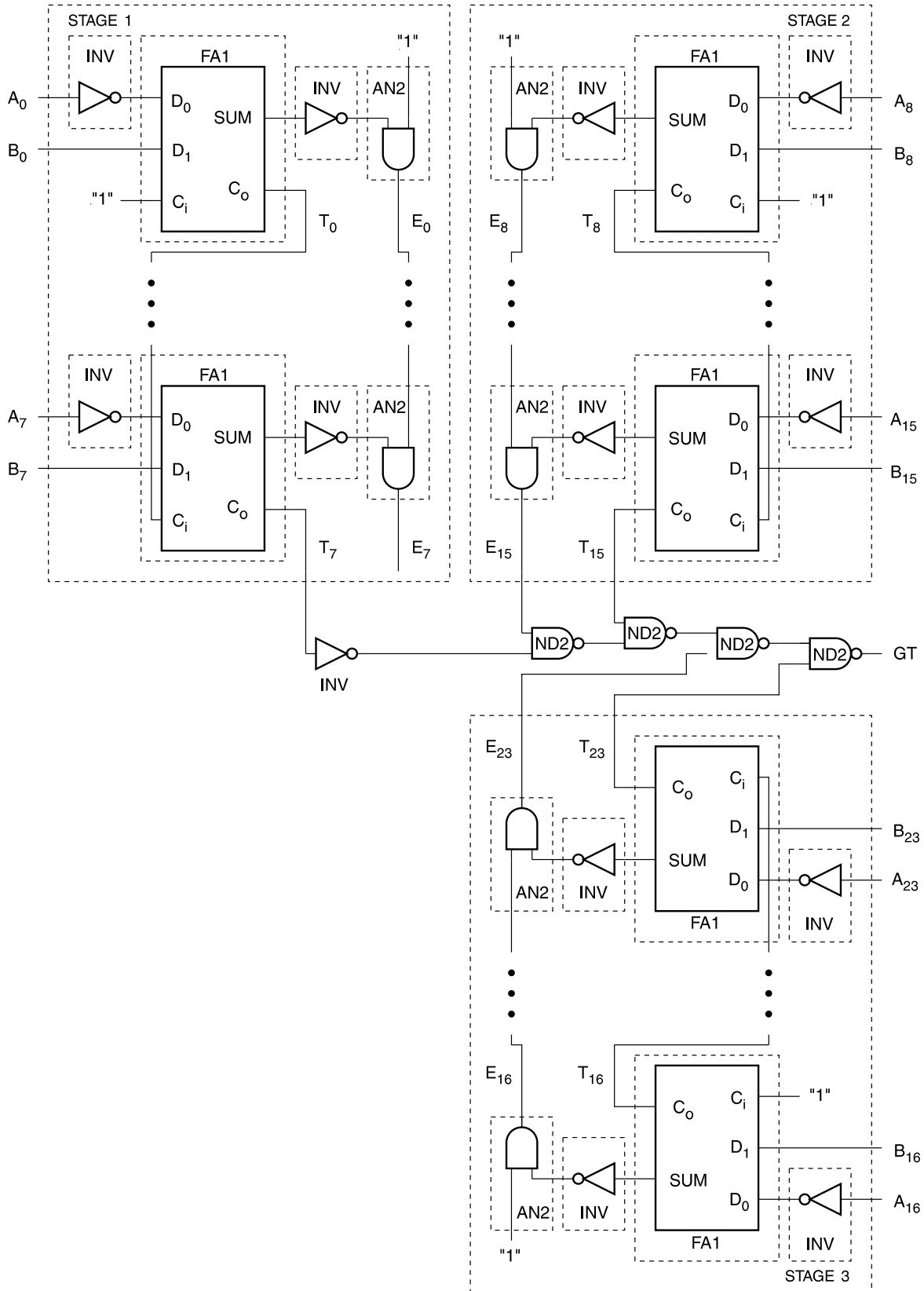


Figure 3. Magnitude Comparator is Composed of Three 8-bit Stages



Precedence in determining magnitude is given to the most significant stage in which the bit portions are different when all other more significant stages have equivalent bit portions. For example, if  $T_{15}$  and  $E_{15}$  become unasserted, which means that the B bits are of greater magnitude than the A bits, and  $E_{23}$  asserts that the A and B bits in its more significant stage are equivalent, then GT will remain unasserted regardless of the results in the less significant stages.

The equations for  $T_n$  and  $E_n$  can be implemented as shown in Figure 2. FA1 is a single bit full-adder macro that is combined with inverters (INV) and two-input AND gates (AN2) to realize the function for  $T_n$  and  $E_n$ . A 24-bit comparator is built as shown in by composing three 8-bit stages and using the  $S_n$  logic to link each stage (Figure 3).

Performance and utilization statistics for the magnitude comparator are given in Table 1. This implementation is available in schematic and layout form.

**Table 1.** Statistics for 24-bit Magnitude Comparator

Comparator	Cell Count <sup>(1)</sup>	Minimum Bounding Box (X × Y)	Wire Cells	Maximum Delay <sup>(2)</sup>
24-bit	246	12 × 33	98	50 ns/20 MHz

- Notes:
1. Includes cells used as wires.
  2.  $A_0 \rightarrow$  GT. Worst-case Commercial Operating Conditions: 70°C, 4.75V.



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