Barrel Shifter

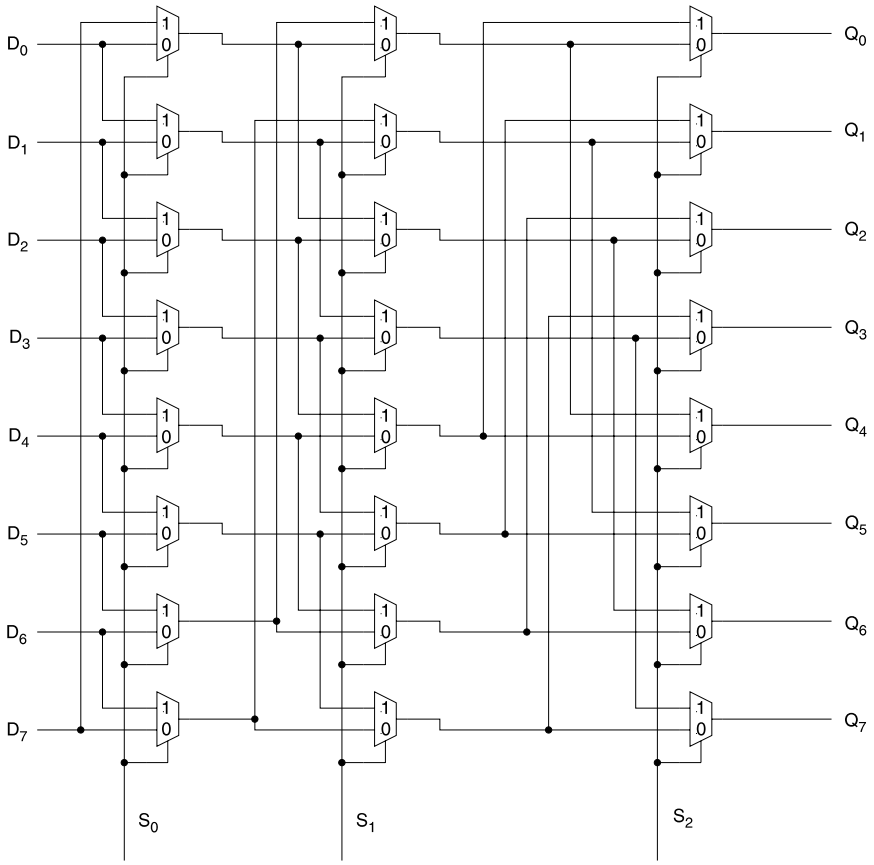
Introduction

The AT6000 Series field programmable gate array (FPGA) allows the designer to implement fast compact 8 bit barrel shifters, and modular shifters that can be easily sized for specific needs. Performance is enhanced by a unique feature of the busing architecture that enables the select control lines to be distributed across the data path with minimal skew, and a cell architecture that allows a two-to-one multiplexer (MUX) to be realized in just one cell.

Description

Figure 1 shows the fast, compact barrel shifter. Depending on the encoded shift control lines, S_{0-2}, the data inputs D_{0-7} are shifted when they reach the outputs Q_{0-7}. If S_0 is asserted and S_1 and S_2 are unasserted, the value at D_{0-7} is passed to the next most significant Q output. For example, D_0 is passed to Q_1, and D_1 passed to Q_2, while D_7 wraps around and is passed to Q_0. If none of the shift controls are asserted, the data inputs D_{0-7} are passed to the corresponding outputs Q_{0-7} without being shifted.

Figure 1. Fast, Compact Barrel Shifter with Encoded Shift Control



Field Programmable Gate Array

Application Note

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Figure 2 shows the modular barrel shifter. The shift line S_{0-6} is coded such that the data is shifted one bit position for every shift line that is asserted. The bit-width and depth of the modular barrel shifter can be easily expanded because of the efficient interconnections network. Each multiplexer output connects to its two nearest neighbors in the next column. The multiplexers on the borders are easily connected via a local bus wire. Bit-slice structures of arbitrary bit-width can be composed and then concatenated to form barrel shifters tailored to specific design needs.

The implementation in Figure 1 is faster because it contains fewer multiplexers. The critical path of the second implementation has more than twice as many MUX cells in series. The delay through a multiplexer cell is 2.7 times the delay through a wire cell, so the delay through three wire cells is approximately equal to the delay through one multiplexer cell. With both implementations being approximately the same size, and the critical paths containing about the same quantity of cells, the path with the lesser amount of multiplexers will be faster.

Figures 1 and 2 reflect the relative physical placement of the logical cells that compose the barrel shifter function and the busing structure that performs the interconnection.

Table 1 gives performance and utilization statistics for both implementations. Both implementations are available in schematic and layout form.

Figure 2. Modular Barrel Shifter with Non-coded Shift Control

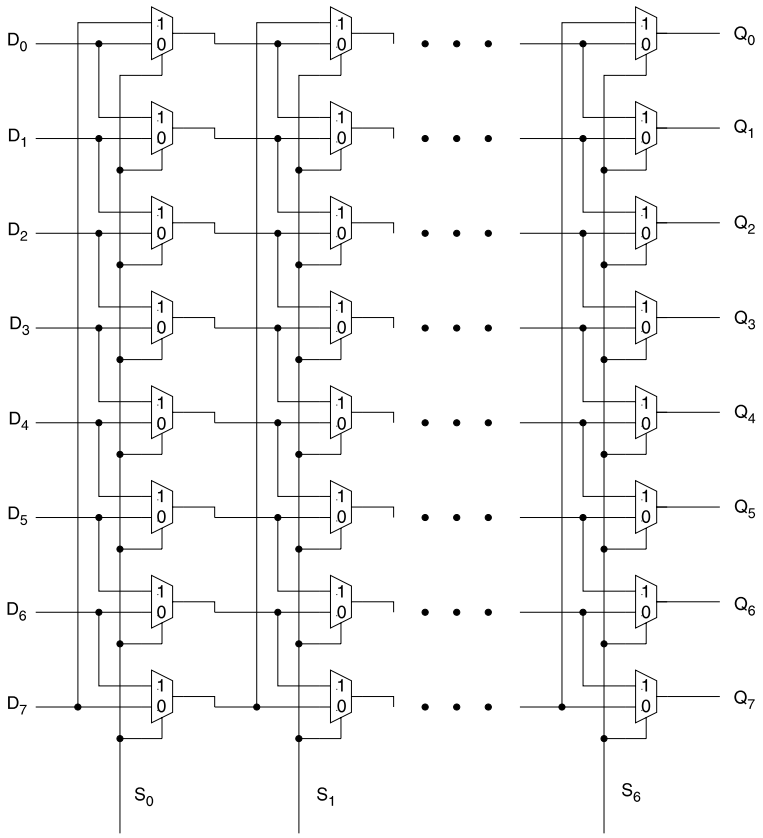

Table 1. Statistics for Barrel Shifter

Version	Cell Count[1]	Minimum Bounding Box (X × Y)	MaximumSpeed[2]
Fast (3 Control Bits, Encoded)	112	8 × 14	28 ns/35.7 MHz
Modular (7 Control Bits, Encoded)	126	13 × 10	44 ns/22.7 MHz

Note: 1. Includes cells used as wires.

2. $D_{0-7} \rightarrow Q_{0-7}$. Worst-case Commercial Operating Conditions: 70°C, 4.75V.

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