Ripple-Carry Adders

Field Programmable Gate Array

Application Note

Introduction

With a NAND and an XOR available simultaneously in a single cell, the AT6000 architecture is ideally suited for implementing arithmetic operations, including parallel adders. Ripple-carry adders – the simplest and most compact parallel adders – require as little as four cells per bit, and one layout has a carry delay of only one cell per bit.

Description

In the AT6000 architecture, a NAND and an XOR – basic building blocks of binary arithmetic – are available simultaneously in a single cell. The NAND/XOR is used in making full adders (FAs), which, in turn, are used in creating parallel adders.

A full adder has three binary inputs – two addends and a carry_in, and two outputs – sum and carry_out. The sum is the exclusive OR (XOR) of the three inputs, while carry_out is the majority (two out of three) of the three inputs. The simplest and most compact full-adder layout in the AT6000 architecture uses just four cells (Figure 1). The carry_in and carry_out, moreover, are aligned so that an *n* bit adder occupying *4n* cells is created by simply abutting *n* full adders. An 8-bit parallel adder constructed from these adders uses only 32 cells (Figure 2).

Figure 1. Full Adder: Compact Layout

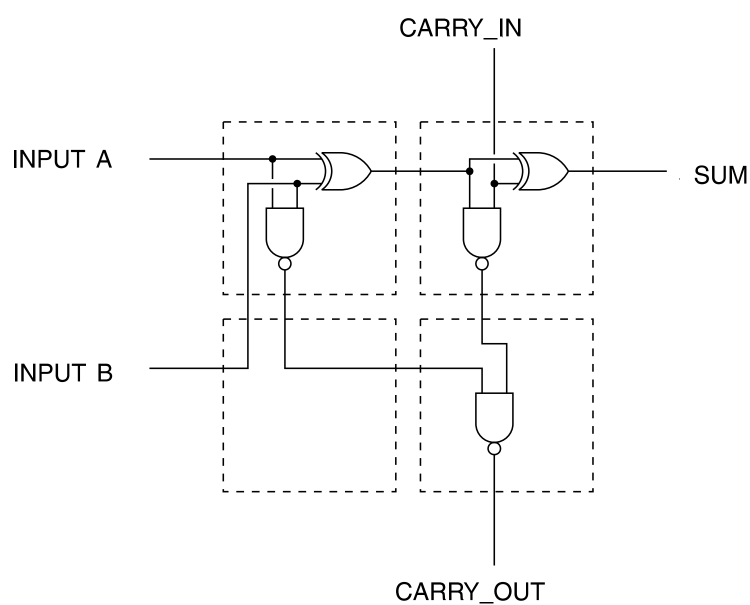

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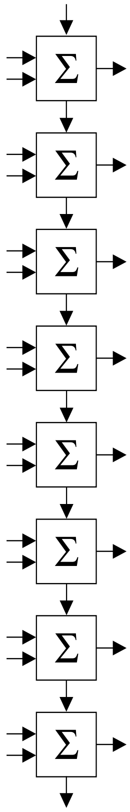
Figure 2. 8-bit Ripple-carry Adder



A second full-adder layout (Figure 3) uses six cells, plus a local bus, but the carry now propagates through only one cell per bit instead of the two cells per bit of the adder in Figure 1. This reduced delay in the carry path produces ripple-carry adders that run about one-third faster. An examination of the circuit shows that the sum output is still the XOR of the three full-adder inputs (the adder has only three distinct inputs and two distinct outputs; the carry_in and carry_out signals are replicated to satisfy the needs of the layout). The carry_out is still the majority of the three inputs although it is now constructed from two AND gates feeding an XOR. A little Boolean algebra shows that the function is identical to the three NAND gates used above (Figure 1) to produce the carry_out.

The size and performance of various ripple-carry adders are summarized below for the -4 and -2 speed grades (Table 1).

Figure 3. Full Adder: Fast Layout

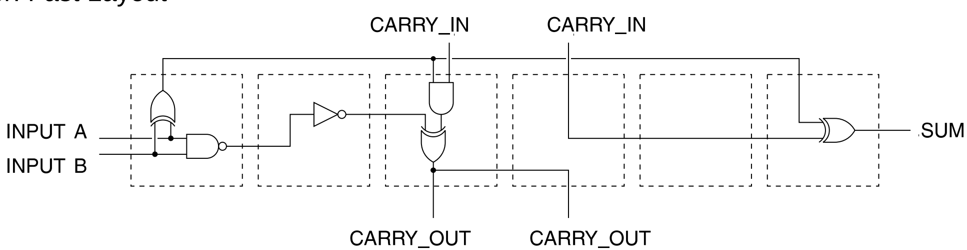


Table 1. Statistics for Ripple-carry Adders

Adder	Cell Count[(1)]	Minimum Bounding Box (X x Y)	Maximum Speed (-4)[(2)]	Maximum Speed (-2)[(2)]
8-bit Ripple Carry	64	2 x 16	59.1 ns/16.9 MHz	35.7 ns/28.0 MHz
8-bit Fast Ripple Carry	48	6 x 16	51.2 ns/19.5 MHz	30.0 ns/33.3 MHz
16-bit Ripple Carry	64	2 x 32	111.9 ns/8.9 MHz	67.7 ns/14.7 MHz
16-bit Fast Ripple Carry	96	6 x 16	87.2 ns/11.4 MHz	51.6 ns/19.3 MHz
32-bit Ripple Carry	128	2 x 64	217.5 ns/4.5 MHz	131.7 ns/7.5 MHz
32-bit Fast Ripple Carry	192	6 x 32	159.2 ns/6.2 MHz	94.8 ns/10.5 MHz

Notes: 1. Includes cells used as wires.
2. Worst-case Commercial Operating Conditions: 70°C, 4.75V.

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