9-bit Programmable Terminal Counter

Field Programmable Gate Array

Application Note

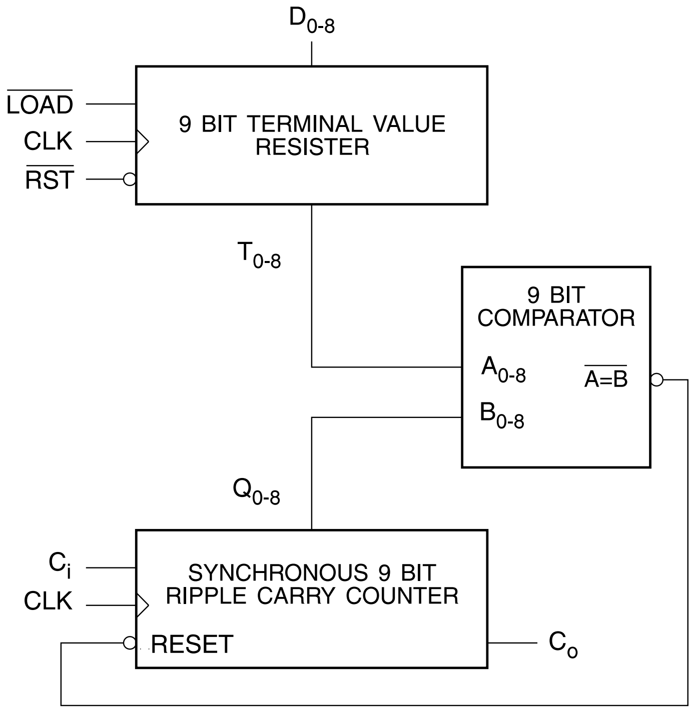
Introduction

The AT6000 Series field programmable gate array (FPGA) lets the designer implement synchronous, programmable 9-bit terminal counters optimized for speed or layout area. A high-performance version is available that can operate at 33 MHz under the worst commercial operating conditions. If layout area is a consideration, a 33% smaller version is available that can still operate at 28 MHz worst case. An additional feature inherent in both counters is the ability to continue counting while a terminal value is being loaded into the terminal register.

Description

Figure 1 shows a block diagram of the counter. Both versions have essentially the same architectural structure. Pin CLK is the clock signal, RST the reset signal, and LOAD the load terminal value signal. CLK is a positive, edge-triggered synchronous signal, RST an active low, asynchronous signal, and LOAD an active low, synchronous signal. Pins D_0 through D_8 are the terminal value inputs, and pins Q_0 through Q_8 are the count bits. Pins C_i and C_o are the carry-in and carry-out signals.

Figure 1. 9-bit Programmable Terminal Counter



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Initial power-up of the AT6000 device resets all the registers in the counter and terminal register. Counting does not commence until a terminal value has been loaded into the terminal register. Any 9-bit value can be loaded into the terminal register through the inputs D_{0-8} by holding LOAD low during the rising edge of CLK. Assuming C_i is asserted, the counter increments on the rising edge of CLK until the terminal value is reached on the outputs Q_{0-8}. On the next rising edge of CLK, the counter is synchronously reset to zero. Figure 2 shows the timing of the terminal value load and count operations for the circuit.

The schematic in Figure 3 shows the detailed implementation of the high-speed version of the circuit. The FDMUX macro is a two-to-one multiplexer that feeds a D-type flip-flop. A terminal value register composed of FDMUX macros lets a terminal value be loaded synchronously through D_{0-8}. The terminal value register holds the previously loaded value at its outputs. Counting does not commence until a non-zero value is loaded into the terminal value register.

A synchronous ripple-carry counter begins counting after a terminal value has been loaded into the terminal register. The counter is composed of FD, XO2, and AN2 macros – D-type flip-flops, two-input exclusive OR gates, and two-input AND gates respectively. Outputs Q_{0-8} feed into a comparator circuit composed of INV inverter gate, X02, and AN2 gates. The output of the comparator controls the initialization of the counter by checking Q_{0-8} against the terminal value. When Q_{0-8} is equivalent to the terminal value, the counter is reset to zero on the next rising edge of CLK.

The critical path of the circuit starts at Q_0, the first bit of the counter, travels through the comparator, and then back to the input of the first counter bit. Performance is enhanced by breaking the chain of AN2 gates in the comparator into three- and four-gate segments (Figure 4), then combining the output of each segment with a two-input NAND macro called ND2. By gating the D-type flip-flops of the counter with the output of the comparator, path delay is minimized and performance is enhanced.

Figure 5 shows the detailed schematic for the compact version. The terminal value register is exactly the same as in the high-speed version, but the outputs of the register are not inverted as they enter the 9-bit comparator. Instead, the outputs of the counter are inverted as they enter the comparator, thus improving layout compactness. An FDXOAN3 macro, a complex gate structure feeding a D-type flip-flop, is used to implement the 9-bit synchronous ripple-carry counter in only nine cells. As in the high-speed version, the critical path also resides in the comparator portion of the circuit.

The performance and utilization statistics for both versions are given in Table 1. Both implementations are available in schematic and layout form.

Figure 2. Timing of Load/Count Operation

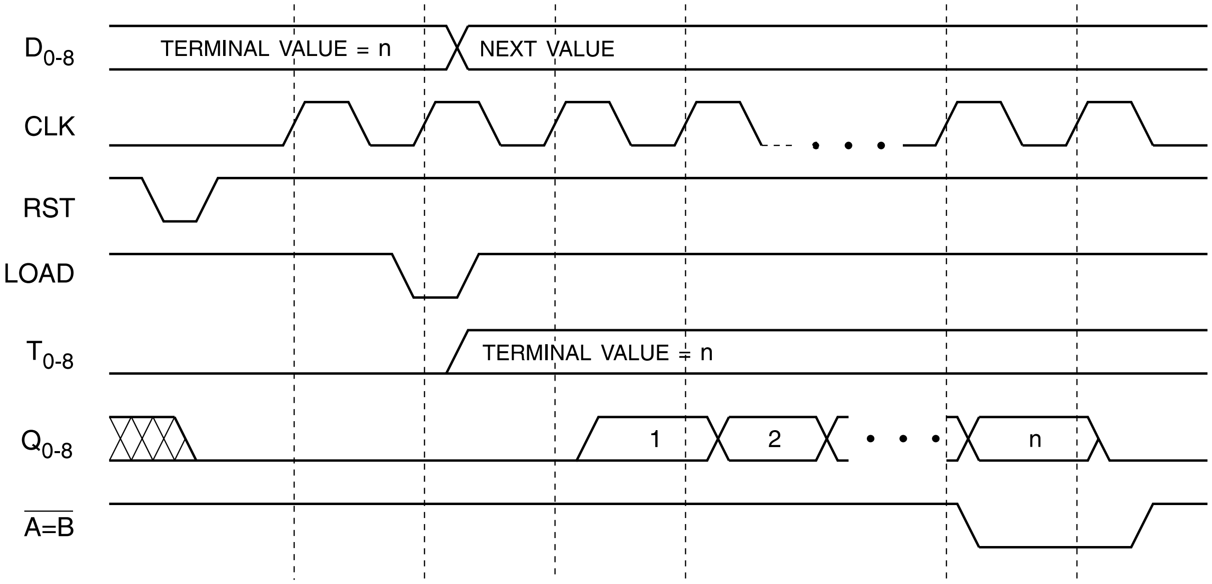

Figure 3. High-speed Programmable Terminal Counter Architecture

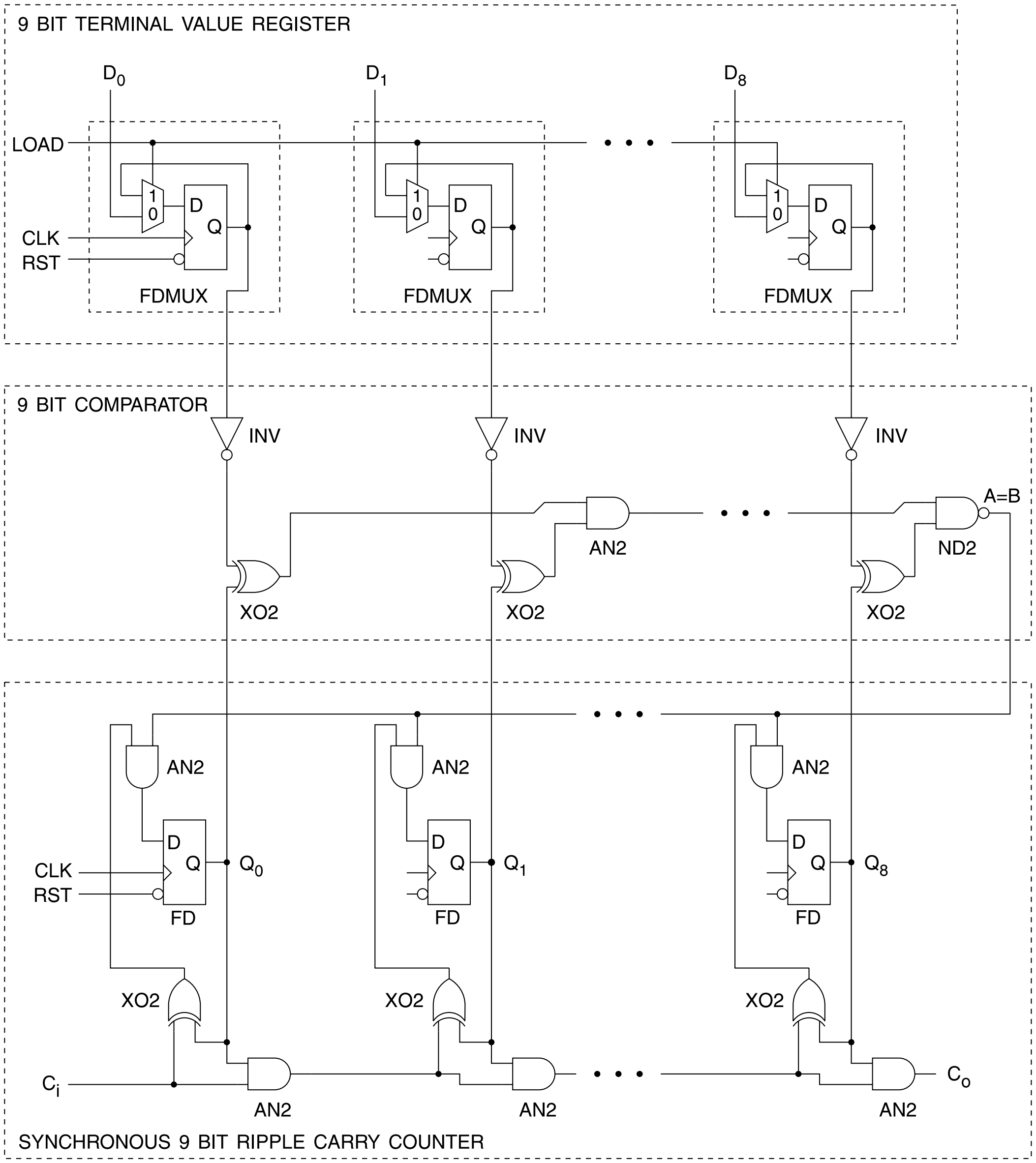

Figure 4. Schematic of Comparator Circuit

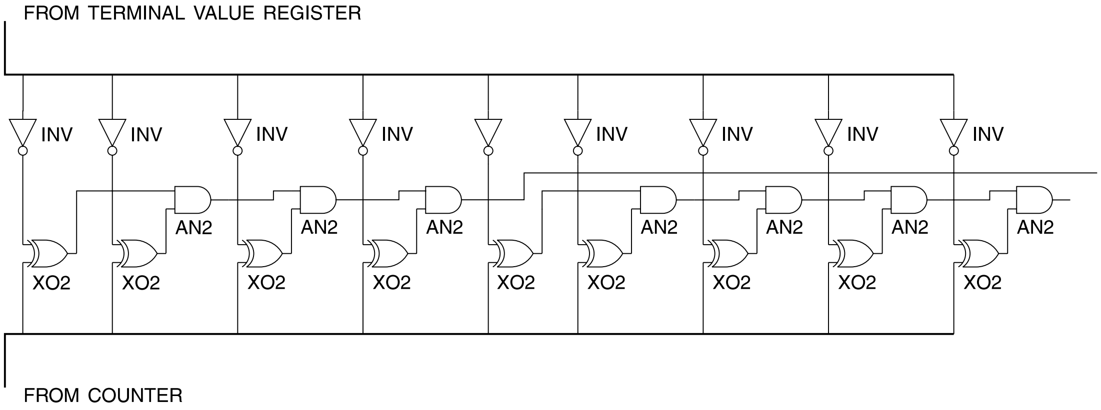

Figure 5. Compact Programmable Terminal Counter Architecture

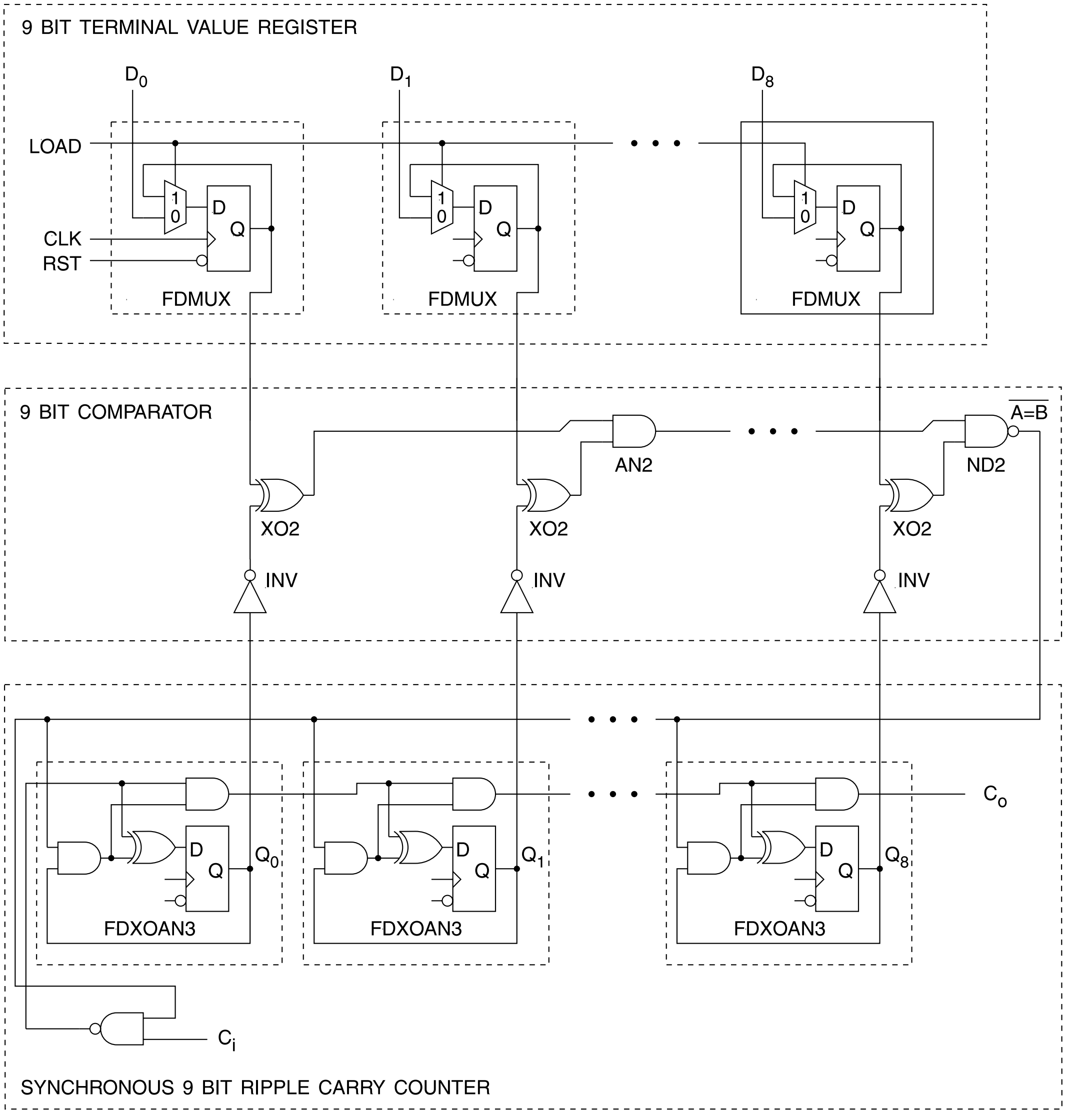

Table 1. Statistics for 9-bit Programmable Terminal Counters

Programmable Terminal Counter	Cell Count[1]	Minimum Bounding Box (X × Y)	Maximum Speed[2]
9-bit (Compact)	69	10 × 7	35.7 ns/28 MHz
9-bit (High-speed)	100	10 × 10	30.3 ns/33 MHz

Notes:
1. Includes cells used as wires.
2. CLK → C_0. Worst-case Commercial Operating Conditions: 70°C, 4.75V.

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