



16-bit Up/Down Counter/Shift Register

Introduction

The AT6000 Series field programmable gate array (FPGA) lets the designer implement a synchronous, 16-bit Up/Down Counter/Shift Register that operates at 22 MHz under the worst commercial operating conditions. In this circuit is most of the combined functionality of the 74193 Up/Down Counter and 74194 Bidirectional Shift Register TTL components. It would take eight discrete TTL components to implement an 16-bit Up/Down Counter/Shift Register. Nearly the same function can be achieved in a AT6005 using less than 8% of the available logic.

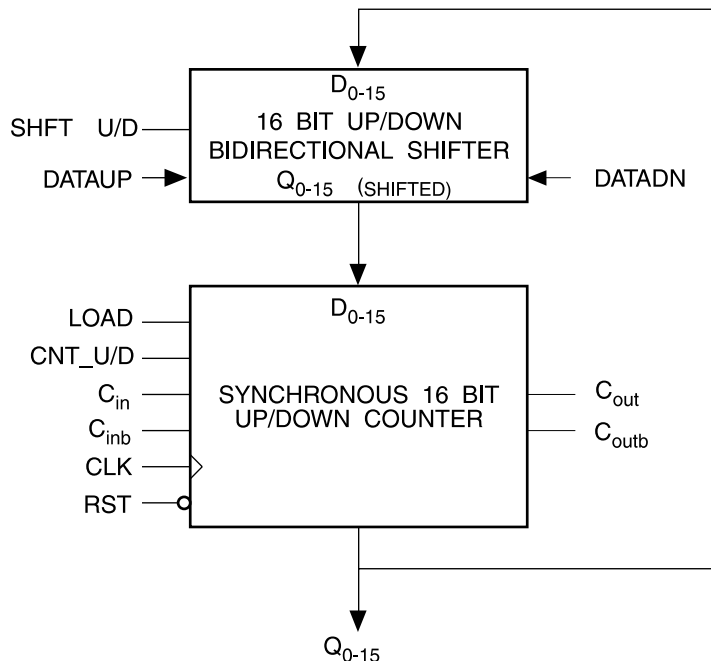
Description

Figure 1 shows a block diagram of the counter/shifter. Pin CLK is the clock signal, RST the reset signal, and LOAD the count/shift control signal. CLK is a positive, edge-triggered synchronous signal, RST an active low, asynchronous signal, and LOAD an active low, synchronous signal. Pins Q_0 through Q_{15} are the count bits. Pins C_{in} and C_{out} are the carry-in and carry-out signals. Pins C_{inb} and C_{outb} are the carry-in borrow and carry-out borrow signals. SHFT_U/D and CNT_U/D control the direction of the shift and count operations. DATAUP and DATADN are the shift-up and shift-down serial data inputs for the shifting operation.

Field Programmable Gate Array

Application Note

Figure 1. 16-bit Up/Down Counter/Shifter



The output of a 16-bit fast ripple-carry counter is input into a bidirectional shifter that shifts the data inputs up or down one bit position. The output of the shifter is fed back to the parallel data inputs (D_{0-15}) of the counter. When LOAD is set high, the output of the shifter is ignored and the counter increments or decrements depending on the CNT_U/D. If LOAD becomes unasserted, the counting operation is inhibited, and the shifter provides the shifted count at Q_{0-15} to the parallel data inputs of the counter. While LOAD remains low, the counter essentially acts as a shift register, and will shift the data at Q_{0-15} either up or down depending on SHFT_U/D.

Initial power-up of the AT6000 device resets all the registers in the counter/shifter. While LOAD and RST are asserted, incremental counting commences if CNT_U/D and C_{in} are asserted before the rising edge of CLK. Decrement counting commences if CNT_U/D is unasserted and C_{inb} is asserted before the rising edge of CLK.

If LOAD is set low, the circuit becomes a shift register on the rising edge of CLK. The CNT_U/D, C_{in} , and C_{inb} signals are ignored, and control of the circuit is determined by SHFT_U/D, DATAUP, and DATADN. If SHFT_U/D is asserted, the data at Q_n will be shifted to Q_{n+1} on the rising edge of CLK. The value present at DATAUP is shifted to Q_0 . Down shifting occurs when SHFT_U/D is set low.

The Up/Down Counter/Shifter must be serially loaded with a starting value.

Although Figure 1 shows that the 16-bit counter has a parallel load capability, the data inputs of the counter are already driven by the shifter. While LOAD is low, counting is inhibited. With the proper control of SHFT_U/D, any

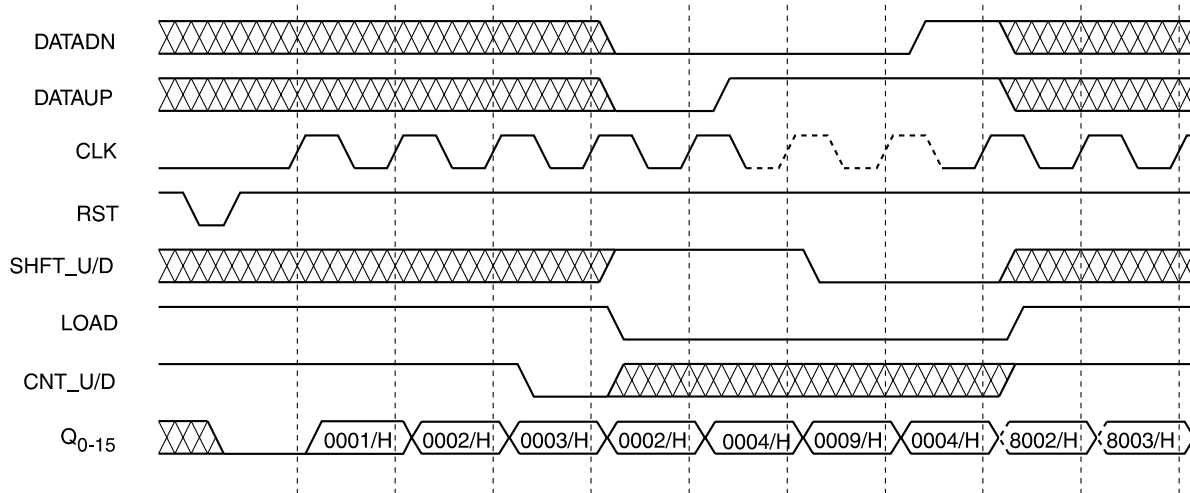
16-bit value can be shifted serially into the register through the inputs DATAUP or DATADN. When the register is loaded with the correct value, Up/Down counting can begin on the first rising edge of CLK after LOAD is set high. Parallel loading of the start value is the only feature not inherent in the circuit that is present in the 74193 TTL device. Figure 2 shows the timing of the count/shift operation.

The schematic in Figure 3 shows the detailed implementation of the circuit. The FDHA macro is a half-adder sum that feeds a D-type flip-flop. Together with the MUX two-to-one multiplexer macros and the SELBUFS selector macros, an Up/Down counter with parallel load is constructed using only six cells per bit. SELBUFS macros enable the carry generation logic for each bit of the counter to be implemented in only one cell. The chain of SELBUFS macros that forms the carry-generation logic is also the critical path of the circuit. In the layout of this counter the least-significant bit Q_0 is distributed to the carry-enable logic of the other more significant bits. Distributing Q_0 will improve the performance by minimizing the delay through the critical path for both up-counting and down-counting.

MUX macros are used to form the shifter portion of the circuit. The inputs into each MUX of the shifter will be the Q_{n-1} and Q_{n+1} outputs of the counter, and the output of the shifter will feed the n th parallel data input of the counter. At the least- and most-significant bits, the MUX macros will use DATAUP and DATADN as inputs.

The performance and utilization statistics for the 16-bit Up/Down Counter/Shifter are given in Table 1. This implementation is available in schematic and layout form.

Figure 2. Timing of Load/Count Operation



NOTE: $C_{in} = C_{inb} = 1$

Figure 3. Schematic of Counter Figure

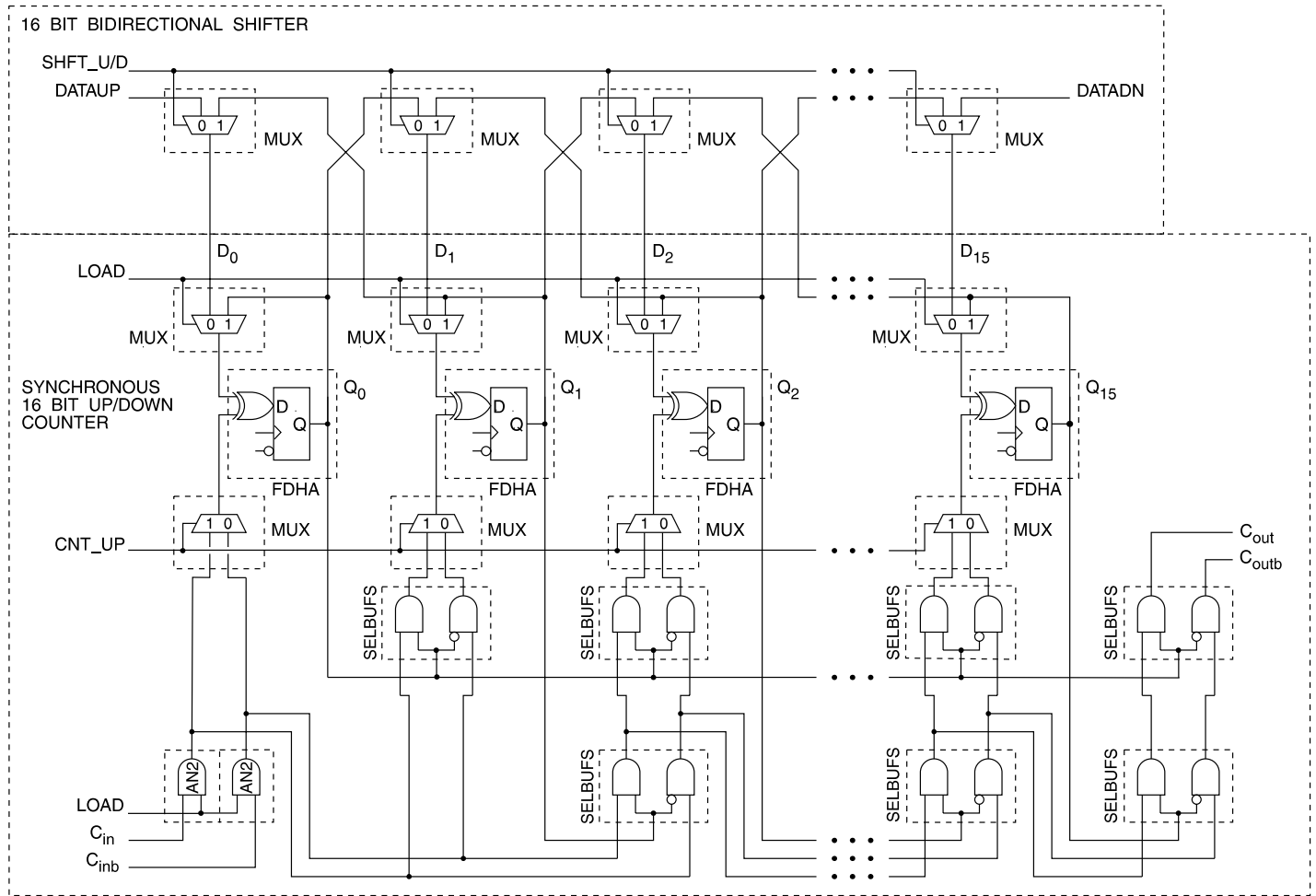


Table 1. Statistics 16-bit Up/Down Counter/Shift Register

Counter/Shift Register	Cell Count ⁽¹⁾	Minimum Bounding Box (X × Y)	Maximum Speed ⁽²⁾
16-bit	215	13 × 18	45.5 ns/22 MHz

Notes: 1. Includes cells used as wires.

2. CLK → C_{out,outb}. Worst-Case Commercial Operating Conditions: 70°C, 4.75V.



Atmel Headquarters

Corporate Headquarters

2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe

Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia

Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan

Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs

1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset

Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand

North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

BBS

1-(408) 436-4309

© Atmel Corporation 1999.

Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

Marks bearing ® and/or ™ are registered trademarks and trademarks of Atmel Corporation.

Terms and product names in this document may be trademarks of others.



Printed on recycled paper.

0465C-09/99/xM