



Compact, Loadable 16- and 32-bit Binary Counters

Introduction

The AT6000 Series architecture accommodates dense, synchronous, loadable binary counters. A 16-bit counter counts at 42 MHz, and a 32-bit at 36 MHz in AT6000-2 devices. Both counters are very compact, yet their inputs and outputs are readily accessible.

Description

Figure 1 is a block diagram representation of the I/O and architecture for a 16 or 32-bit counter. Pin CLK is the clock signal, RST the reset signal, and LOAD the load data signal. CLK is a positive, edge-triggered synchronous signal, and LOAD is an active low, synchronous signal. Pins D_0 through $D_{15,31}$ are the load

data inputs, and pins Q_0 through $Q_{15,31}$ are the count bits. Pin C_i is the carry in; C_o is the carry out.

4-bit synchronous loadable binary counters are used to compose larger 16 or 32-bit counters. These 4-bit counters toggle on the rising edge of CLK when their RST is high and LOAD is low.

Initial power-up of the AT6000 device resets all the registers. The counter begins counting on the first rising edge of CLK if C_i and RST are set high and LOAD is set low. The circuit counts by allowing each 4-bit counter stage to toggle in succession on the rising edge of CLK if the Q outputs of all prior stages are asserted. Asserting RST at any time inhibits counting, but also resets the 4-bit counters to low values.

Figure 1. Architecture and I/O of 16-bit or 32-bit Counter

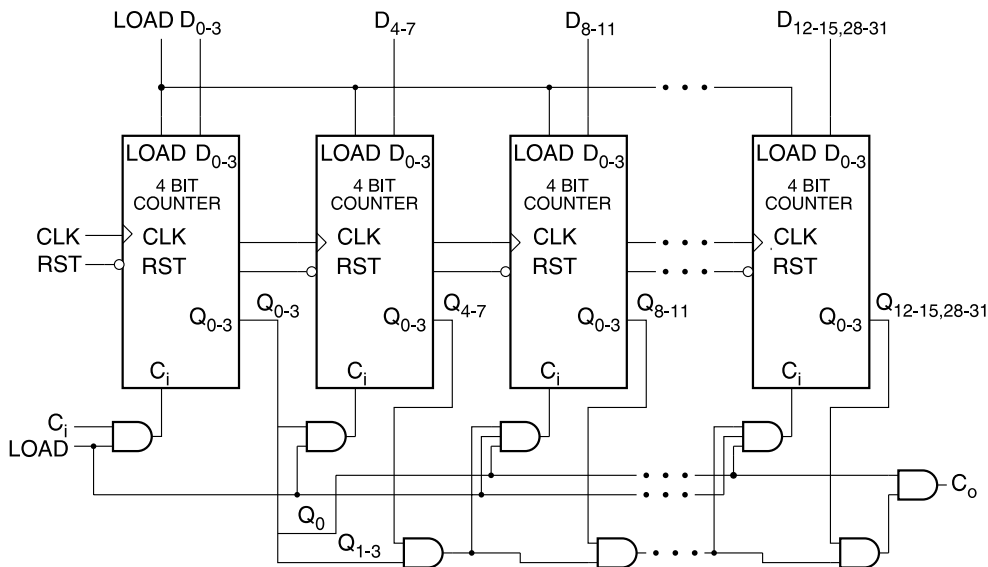


Figure 2 shows the implementation of the 4-bit counter stage used in the 16- and 32-bit counter architectures. A Q output in this circuit will toggle if C_i is high and LOAD is low, and all prior Q output are asserted upon the rising edge of CLK. If C_i and LOAD are low, then Q will not change. This circuit exists as a predefined marco library element called CRP4.

To load a value into a 16-bit counter, LOAD is set high prior to the rising edge of CLK. The value is latched into the CRP4 stages on the rising edge of CLK.

LOAD should then be held low until after the next rising edge of CLK to allow the carry-enable logic time to recalculate the carry-enable bit for each CRP4 stage. The carry-enable logic is the chain of two-input AND gates that generates the C_i signal inputs for each CRP4 stage. In Figure 3, if LOAD is asserted for two clock cycles the data at D_{0-15} is

loaded into the CRP4 macros on the first clock cycle, and counting continues from the newly loaded value two cycles later

During the LOAD cycle, when the data at D_{0-15} is clocked into the 16-bit counter, the carry-enable logic must have time to generate and propagate the results to every bit. Since an arbitrary number at D_{0-15} can cause a carry-enable signal to propagate along the entire length of the carry-enable chain, the critical path during a LOAD operation has the potential to pass through 17 AND gates (AN2) before entering the last register element. By holding the LOAD signal low an extra clock cycle to inhibit the counting operation (as shown in Figure 3), the carry-enable logic will have additional time to propagate the correct values to each bit.

Figure 2. Schematic of a 4-bit Counter Macro CRP4

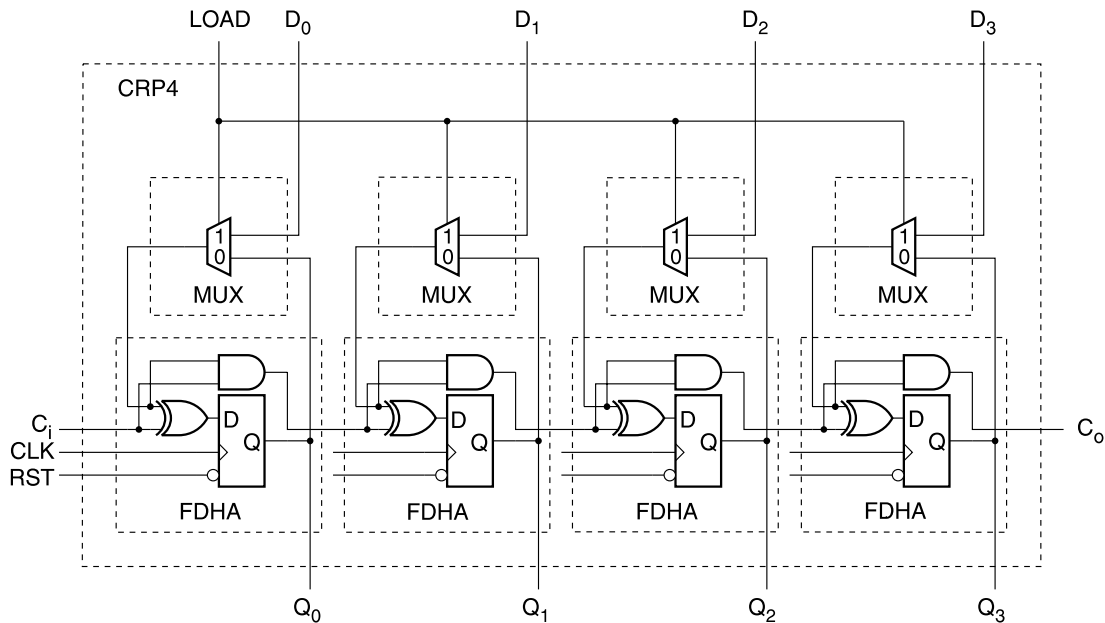


Figure 3. Timing Diagram of Counter Load Cycle

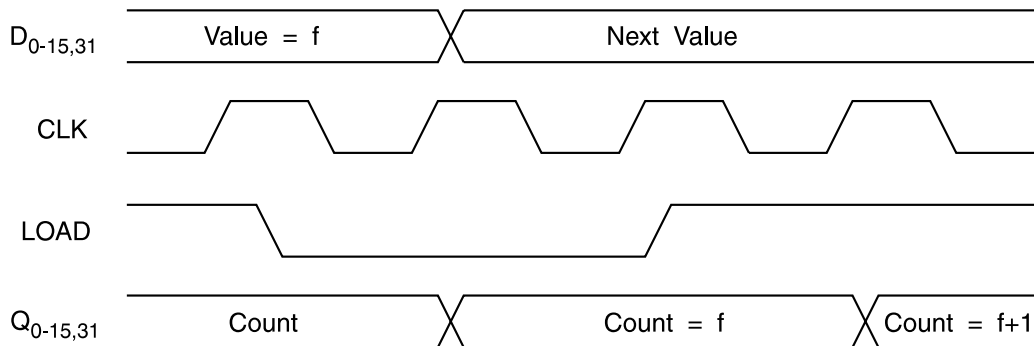


Figure 4 shows the detailed schematic of a 16-bit counter partitioned into four stages. During normal operation Q_0 , the least-significant bit of the counter, is also a fast carry-enable signal. All bits greater than Q_0 must wait for Q_0 to switch logic levels before their carry-enable logic stabilizes. Q_0 is distributed to all four CRP4 macros in an attempt to balance and minimize the propagation delay of Q_0 to the C_i of the more significant CRP4 macros. For example, as the more significant bits in the first stage are asserted, their values trickle through the two-input AND gates (AN2) that form part of the carry-enable logic. When all the more sig-

nificant bits are asserted and Q_0 switches from low to high on the rising edge of CLK, the carry-enable signal to the C_i input of the second CRP4 is enabled. While its C_i signal is asserted, the CRP4 in the second stage counts on the rising edge of CLK.

By replicating and concatenating the circuitry surrounded by the dotted box, larger counter functions are realized. The performance and utilization statistics for the 16- and 32-bit counters are given in Table 1. Both implementations are available in schematic and layout form.

Figure 4. Schematic of Counter Architecture

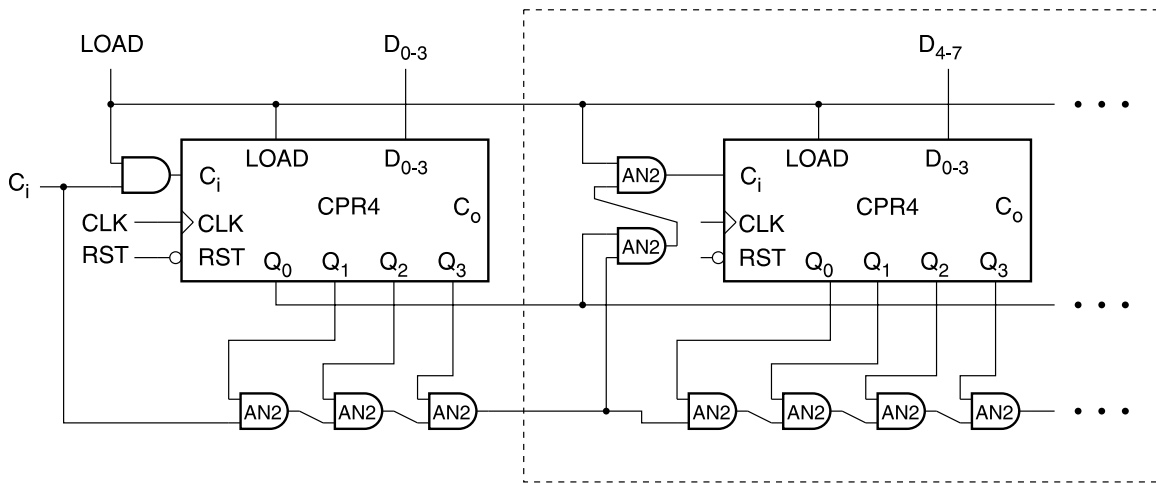


Table 1. 16- and 32-bit Counter Performance Comparison

Counter	Cell Count ⁽¹⁾	Minimum Bounding Box (X × Y)	Maximum Counting Speed ⁽²⁾	Maximum Loading Speed ⁽³⁾
16-bit	76	10 × 8	22 ns/45 MHz	55.5 ns/18 MHz
32-bit	136	18 × 8	35.7 ns/28 Mhz	83.3 ns/12 MHz

- Notes:
1. Includes cells used as wires.
 2. Worst-Case Commercial Operating Conditions: CLK → C_0 , 70°C, 4.75V.
 3. Worst-Case Commercial Operating Conditions: LOAD → $Q_{0-15,31}$.



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