
Data Acquisition Systems Using Cache Logic[®] FPGAs

Atmel has developed an enabling technology to make adaptive hardware possible for data acquisition, logic analyzer, and other instrumentation products. This capability, trademarked as *Cache Logic*, was developed and patented by Atmel Corporation.

Cache Logic is conceptually similar to cache memory. In cache memory, the highest speed memory (usually SRAM) is used to store active data, while the bulk of data resides in lower cost storage, such as DRAM, EPROM, disk, etc. Cache Logic works in a similar fashion. Only a small fraction of the circuitry is active in a system at any given time. Only active functions are loaded into the logic cache, while unused functions, or variations, reside in lower cost system memory. It is even possible to compile variations of a design in real time. Logic functions are loaded into the logic cache as required, replacing, or complementing the logic already present.

The ability to implement cache logic requires FPGAs that are capable of being dynamically reconfigured in-system, either completely or partially, without disrupting the operation of the balance of logic in the device. Another requirement is architecture symmetry. This is necessary to enable the arbitrary placement of generic blocks in a location that is available as required. It is also necessary to allow for easy modeling of device characteristics for the artificial intelligence required in the partitioning of a design. The symmetry also simplifies the creation of arrays of devices to create a larger digital medium for the implementation of cache logic. Cache Logic can be used in many applications.

The example used in this description of cache logic will be a series of data acquisition products. The example will also discuss the concept of virtual products, which utilize the flexibility of programmable logic. Virtual products do not require cache logic programmability, but as we see the use of cache logic greatly reduces the amount of programmable digital media needed to implement a virtual product.

The Virtual Product

A *virtual product* is a combination of a "tangible asset," such as a data acquisition board and a service, such as product customization. The first thing to understand about virtual products is what the end customer wants, and how manufacturers can match their core competencies with these needs.

There are two issues raised in the manufacture of virtual products:

1. How to balance economy of scale achieved in volume manufacturing with special features that customers are willing to pay for; and
2. How to create diversity while maintaining a level of quality associated with standard high-volume production.

Cache Logic and FPGAs help the manufacturers achieve these two requirements of virtual products. A virtual product line is one that has characteristics that meet the needs of a class of customers. An example would be a PC based data acquisition product. Such a product has certain physical requirements consistent with a PC bus card standard. The board would also



Field Programmable Gate Array

Application Note



have a series of standard data gathering features, such as multiple channel A-to-D converters, digital I/O ports, D-to-A converters, and high-speed clock counters. These features are implemented in standard, high integration ICs. The most complex portions of these products are the data path and protocol sections that connect the PC to the standard ICS products. The structure of this data path is a function of optimizing system performance, cost, and customer preference.

The traditional approach to creating data-acquisition products is to create a board with a standard bus footprint, use industry standard A-to-D and D-to-A circuits, and then create a custom data path. The manufacturer then has to trust marketing studies and instinct to determine the best data path approach. It is possible to hedge the bet by adding redundancy. This redundancy has two detrimental effects: added cost, and added complexity for the end user. The selection of wrong data path protocol or excessive complexity caused by redundancy results in dissatisfied or nonexistent customers.

A virtual product does not mean that a manufacturer would be able to offer one product that was all things to all people. The use of programmable logic would allow a manufacturer create an extensive catalog of products, but only have a small number of tangible assemblies to tool for manufacturing. The manufacturer would use FPGAs and cache logic FPGAs to create diversity in their product line. The cost of diversity to the manufacturer is the cost of service, or "personalization engineering", required to create a niche design on a standard assembly. The advantage for the customer is a mass produced product that meets their specific needs.

Quality

Quality is a very important advantage of the virtual product approach to design. Quality is usually the ultimate factor in device selection. Quality customer service can be defined as a high level of product diversity, and is measured by the degree that the specific customer requirements are met.

The foundation of product quality is in the manufacturing process. Unlike service quality, product diversity (quality customer service) is detrimental to the goal of 100% quality. Total product quality is attained by tooling for a long term process of implementation, evaluation, and feedback. Multiple custom products produced on the same assembly line conflict with the ability to attain the highest product quality and best economies of scale. Quality enhancing techniques, including just-in-time delivery, multi-discipline staffing, and integrated engineering, do not work well with multiple short run products.

The virtual product approach allows a manufacturer to perfect a single assembly. The FPGA's ability to be configured for self-test could even enhance quality of the assembly. Atmel has developed the IEEE1148 boundary scan super-macro. Utilizing the reconfigurable logic capability of the AT6000 family, the boundary scan function may be loaded into the device, diagnostics performed, and then the device can be reconfigured for other logic functions. A single Atmel device may be used for testing and logic, with no overhead or speed penalty, as is the case for all other FPGAs and other ASIC devices.

The result would be an inventory of nearly identical raw product assemblies, which through virtual design becomes a catalog full of products when shipped to the customer. Most customer problems can be traced back to the virtual design personalization process, and be repaired in the field with FPGA configuration updates. It is also possible to introduce new features into virtual products as soon as they are conceived, rather than wait until a new hardware product is designed.

A New Paradigm in Customer and Supplier Relations

New ways of doing business will develop between suppliers and their customers in a "virtual product world." The customer must realize that the cost of product development is amortized in the customized virtual product. The cost of a new personalization may be nearly the same as a complete product.

A virtual product is obsolete when the need for a personalization ceases to exist, as opposed to when the product assembly wears out.

Data Acquisition Example

The Data Acquisition system shown in the accompanying figure is one where a family of products is desired but only one assembly will be manufactured. The intent is to offer a Multiple Channel Analog-to-Digital conversion and 16 digital I/O channels, and multiple digital timers for setting sample periods. The product will be a PC-AT bus card that supports various combinations of data transfer protocols. It is conceivable that different classes of customer will want use a specific setup exclusive of all others, and not understand why anyone would want to work any other way. Putting the features into a matrix shows how many potential products are possible from this set of components (see Table 1).

Table 1. ADC or Digital I/O Sample Mode

Bus Interface	External	Timer	Demand	State	Continuous
I/O Mapped	X		X		X
I/O with Internal	X	X		X	X
DMA Byte Transition	X	X	X	X	X
DMA Array Transition		X	X	X	X

The result is over 16 products that are different in their data path and protocol approach. It is possible that all of these protocols and data path structures can be implemented in a single 2,000- to 5,000-gate FPGA. Cache Logic makes the fitting of the protocol in 2,000 to 5,000 gates possible. This is because each data path protocol combination still needs to be programmable. Items such as timer periods, I/O direction and grouping, the use of each interrupt and timer output, and DMA address counters can be implemented using cache logic, saving circuit redundancy and complexity.

Timer Periods

The timers can be compiled in a structured format. The user defines the number and period of timers required. Each timer contains an N-bit counter, and an M-value decoder, where M is the count equal to the desired period. The Atmel symmetric architecture makes the creation of macros from a high level description straight forward. An area for timers is included in the FPGA. The configuration data for that area is compiled according to customer description. The customer would receive a compiler program, and not a set of pre-defined configuration.

I/O Direction

The FPGA has flexible, individually programmable I/O. There is no reason that a description of the I/O direction and byte grouping could not result in the appropriate configuration of that area of the FPGA. The grouping of the I/O's into bytes is made by a cross-point switch. The cross-point switch is implemented using FPGA programmability. The only requirement in the development of the product is the allocation of sufficient resources in the FPGA for the cross-point area. A byte grouping description by the user would then result in configuration information for enabling the proper pass gate connections in that section of the FPGA.

Timer and Interrupt Usage

In a data acquisition circuit interrupts and timer outputs are used by many parts of the circuit. Time is required to set the period of a digital or analog sample. As the digital I/O

control function, the interrupt and timer outputs can be routed to various combinations of control inputs, PC bus or internal logic of the data acquisition chips. This flexibility, although like a cross-point switch, would be more of a channel routing function. A set of routing resources is used for the connection of various programmable inputs and outputs with access to the reserved channel area.

DMA Address Generation

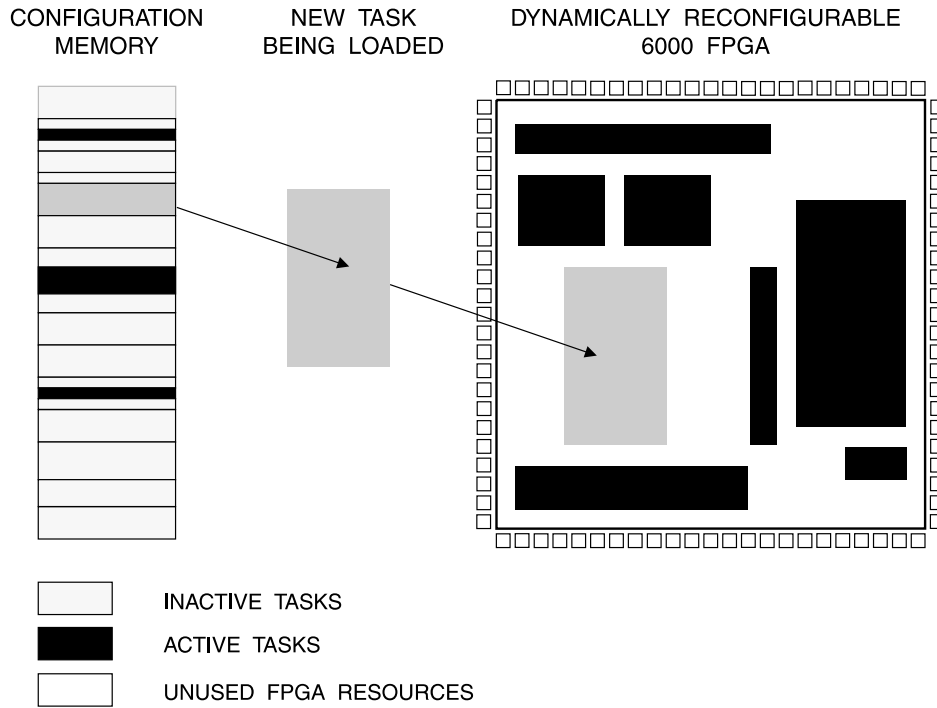
In designs using DMA, the DMA address is stored in a register or counter, depending on the mode. This counter is compiled based on software requirements.

FPGA Configuration

Figure 1 shows the configuration of the FPGA SRAM: controlling its functionality and hookup are a patchwork of configuration information from various sources. Some are a base configuration file used by all products, others from look-up tables or macro compilers. The Atmel FPGA would allow items such as timer periods, or DMA address values to be updated continuously, without effecting the operation of unrelated logic. The advantage of cache logic is the elimination of redundancy. Cache Logic allows the creation of any structure from the digital medium. In traditional designs a circuit would have redundancy for each anticipated eventually, and the control to enable and disable it as well. Even if an application used all possible features, some circuits would be idle, since some combinations would never occur concurrently.

The creation of FPGA configuration files from a high-level description is not an easy task. The manufacturer of a virtual product will need to make the description of the final configuration as intuitive as possible for the end customer. Given equal raw product assemblies the virtual product, like the fixed product that is easiest to use, will be the most successful. The FPGA manufacturer's responsibility is to the manufacturer. The FPGA configuration and architecture must be easy to grasp, and the configuration process must be readily available. A set of compilation development tools and example like this data acquisition product will help to make the manufacturer more comfortable with the implementation of cache logic designs.

Figure 1. Cache Logic Concept



Benefits

There are several benefits of this approach to data-acquisition and other instrumentation suppliers:

1. New functionality may be added to existing hardware, without having to make modifications to the board.
2. The hardware may be tailored to the application, resulting in higher system performance across a broad range of applications.
3. Overall system reliability is improved by reducing the number of physical products and utilizing boundary scan macros for manufacturing and system testing.
4. Overall product life cycle costs are significantly reduced by using reusable software and hardware:
 - Lower development costs
 - Lower inventory costs
 - Quicker time to market
 - Fewer parts on the board
 - Lower power consumption
 - Lower total system cost

Summary

To many people the ideal of a virtual product is a futuristic concept. The FPGA of today is a virtual product. It is available and dependable. The Atmel FPGA and its abilities to implement cache logic make it a foundation for other virtual products. Design with this new technology has been commercially demonstrated. Today's design methodology, that requires a new product for each new function, will be replaced by the virtual product. The needs of both customers and suppliers, with customized products and improved quality; while reducing product development time and cost and attaining economies of scale by high volume production.



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