
AT6000 Series Configuration

Configuration is the process of loading a design into an AT6000 Series Field Programmable Gate Array (FPGA). AT6000 Series devices are SRAM-based and can be configured any number of times. The entire device or select portions of a design can be configured. Sections of the device can be configured while others continue to operate undisturbed.

Configuration data is transferred to the device in one of six modes. Full configuration takes only milliseconds. Partial configuration takes even less time and is a function of design density.

Configuration is controlled by dedicated configuration pins and dual-function pins that double as I/O pins when the device is operating. Three pins, M0, M1 and M2 determine the configuration mode (Table 1). The number of dual-function pins required for each mode varies (Table 2).

Mode 4 is automatically initiated after power-up reboot; the others are initiated by the user. Configuration data can come from a variety of external logic sources, including a PC parallel port, microprocessor, EPROM or EEPROM Serial Configuration Memory (AT17C128).

The user determines the configuration mode for loading the bit pattern into the device. The Integrated Development System software generates the SRAM bit pattern required to configure an AT6000 Series FPGA. Many factors can influence the user's choice of configura-

tion mode, including device size, board space, required configuration speed, number of devices to be configured, and design size.

This document suggests guidelines for device configuration and describes each of the configuration modes in detail.

A basic understanding of the device architecture, as described in the AT6000 Series data sheet, is assumed.

Features

Variety of Formats

- PC Parallel Port
- Microprocessor
- Serial/Parallel EPROM
- Serial/Parallel EEPROM

Configuration Windows

- Full or Partial Reconfiguration
- Bit-stream Compression Algorithm

Reprogrammable

- Download Configuration any Number of Times
- Reconfigure In-System Down to Cell Level

Fast

- Full Configuration: 1-8 Milliseconds
- Partial Configuration: 0.2 μ s/Cell



Field Programmable Gate Array

Configuration Guide



Table 1. AT6000 Series Configuration Modes

Mode	Description	M2	M1	M0	Application
0	Configuration Reset	0	0	0	Reset used for soft reboot ⁽¹⁾
1	Address Count-up, External CCLK	0	0	1	Fast Configuration; Parallel EPROM
2	Address Count-down, External CCLK	0	1	0	Fast Configuration; Parallel EPROM
3	Bit-sequential, External CCLK	0	1	1	Serial Communication Port to UART
4	Bit-sequential, Internal CCLK	1	0	0	Serial EPROM; Auto Configuration
5	Address Count-up, Internal CCLK	1	0	1	Parallel EPROM
6	Byte-sequential, External CCLK	1	1	0	Parallel Port of Microprocessor

Note: 1. This should NOT be used during initial powering (POR) of the device.

Configuration Modes

Powering up an AT6000 Series FPGA is a three-step process. When power is first applied, the device enters an initialization state that takes up to 16 milliseconds and resets the SRAM to all zeros. Cells in the array become cross wires with no A or B inputs selected, all bus drivers are switched off, repeaters are disabled, I/Os are set as TTL inputs with the pull-up enabled, column clocks are set to “0,” and column resets are set to “1.”

After initialization, the device enters the configuration state and writes to the memory bits that control cell functionality and interconnection.

Seven configuration modes are available:

- Mode 0: Configuration Reset
- Mode 1: Address Count-up, External CCLK
- Mode 2: Address Count-down, External CCLK
- Mode 3: Bit-sequential, External CCLK
- Mode 4: Bit-sequential, Internal CCLK
- Mode 5: Address Count-up, Internal CCLK
- Mode 6: Byte-sequential, External CCLK

Mode 0 is not a true configuration mode because it does not load a design into the FPGA. Instead, mode 0 initiates the reboot sequence and clears the device, preparing it for reconfiguration.

Modes 1, 2 and 5 generate external address outputs so the user can conveniently access sequential data from a standard parallel EPROM. The generated output addresses bear no relation to the internal addresses of the FPGA’s configuration SRAM, they simply count up or down with each CCLK edge to create a sequential byte stream. Mode 6 is similar to modes 1, 2 and 5 but assumes a system-generated bit stream and does not generate external address outputs. Modes 3 and 4 use a serial bit stream received from the system, an industry-standard EEPROM

(AT17C65/128/256) or the download cable provided with the Integrated Development System. The data in each byte is serialized with the least-significant-bit supplied first. Mode 4 can be initiated automatically by the FPGA with the AT17C65/128/256 Serial Configuration Memory.

Modes 3 and 4 will typically be the most popular configuration modes because they require the fewest pins and receive data from serial EEPROMs that take up minimal board space.

Pins Used for Configuration

AT6000 Series FPGAs have three kinds of pins: dedicated I/O pins, dedicated configuration pins, and dual-function pins which act as I/O during operation but are used for various control signals during configuration. (For more on device pins refer to the AT6000 Series data sheet.)

Dedicated Configuration Pins

There are six signals dedicated to programming: M0, M1, M2, CCLK, CON and CS.

M0, M1, M2

The mode pins are inputs that determine the configuration mode to be used. Table 1 (this page) lists the states for each configuration mode. M0, M1 and M2 can be fixed in modes 1 through 6 and ignored. Mode 0, configuration reset (soft reboot), can be initiated by asynchronously by holding CON and CS Low, and driving M0, M1, and M2 Low. After holding this condition (t_{PUZ}), the mode pins should be returned to the proper mode selection value to start the configuration. The device should not be powered up in mode 0; mode 0 is for soft reboot only.

Table 2. Dual-function Pin Usage

Mode	Minimum Dual-function Pins	Optional Dual-function Pins	A0-16 Outputs	D0 Input	D1-7 Inputs	$\overline{\text{CHECK}}$ Input	$\overline{\text{ERR}}$ Output	$\overline{\text{CSOUT}}$ Output
0	0	0	N	N	N	N	N	N
1	25	4	R	R	R	O	O	O
2	25	4	R	R	R	O	O	O
3	1	3	N	R	N	O	O	O
4	1	3	N	R	N	O	O	O
5	25	4	R	R	R	O	O	O
6	8	3	N	R	R	O	O	O

Note: N = Not used, R = Required, O = Optional

CCLK

CCLK is the configuration clock signal. It is an input or an output depending on the mode of operation. In modes 1, 2, 3 and 6 it is a TTL input, in modes 4 and 5 it is a CMOS output with a typical frequency of 1 MHz. In all modes, the rising edge of the CCLK signal is used to sample inputs and change outputs.

$\overline{\text{CON}}$

$\overline{\text{CON}}$ is a bidirectional open-collector pin that provides the configuration control and status signal. Configuration starts on the first CCLK edge when $\overline{\text{CON}}$ is driven and held low. Configuration continues until $\overline{\text{CON}}$ is pulled high by a pull-up or by the configuration system. $\overline{\text{CON}}$ is driven low by the device until configuration is complete. The device moves to the operation state on the first CCLK edge after $\overline{\text{CON}}$ is high.

$\overline{\text{CS}}$

$\overline{\text{CS}}$ is the configuration chip select pin. $\overline{\text{CS}}$ must be low for configuration to occur. Pulling $\overline{\text{CS}}$ high during configuration does not stop the process, but the pin should be held low throughout configuration. $\overline{\text{CS}}$ can be used to cascade devices (see Figures 9 and 14) and create an addressed, multiple-device programming system (see Figure 15).

Dual-function Pins

Dual-function pins are programming pins during configuration and I/O pins during operation. The number of dual-function pins used during configuration varies from mode to mode. Some dual-function pins act as configuration status pins and are optional regardless of mode. The optional pins are most useful when cascading devices to program multiple FPGAs from a single data source. Table 2 (above) lists the dual-function pins used with each mode.

D0-D7

D0-D7 are data input pins. Parallel modes 1, 2, 5 and 6 use all eight data inputs, serial modes 3 and 4 use only one, D0.

$\overline{\text{A0-A16}}$

A0-A16 are address output signals, used by modes 1, 2 and 5, to drive an EPROM or other external addressed-memory device.

$\overline{\text{CSOUT}}$

$\overline{\text{CSOUT}}$ drives $\overline{\text{CS}}$ of the next device in a configuration chain.

$\overline{\text{CHECK}}$

$\overline{\text{CHECK}}$ is an input that enables an internal SRAM checking feature when used without B3 of the Configuration Control Register.

$\overline{\text{ERR}}$

$\overline{\text{ERR}}$ is an output that switches low when an error is detected. It is used with the $\overline{\text{CHECK}}$ function, or when protocol errors occur during configuration. $\overline{\text{CHECK}}$ and $\overline{\text{ERR}}$ work together to perform simple and advanced diagnostic tests. For example, they can be used to verify the accuracy of a configuration run. With the $\overline{\text{CHECK}}$ pin low, download the configuration file a second time. The device systematically compares the data values in the configuration file with the data already programmed into the device's SRAM. If a mismatch is found, the $\overline{\text{ERR}}$ pin switches and remains low until the end of the configuration cycle.

Pin Status

The status of dual-function pins is determined by the device state. All I/Os are disabled during initialization. To move from the initialization state to configuration, the $\overline{\text{CON}}$ and $\overline{\text{CS}}$ pins are driven low. During configuration, the dual-function pins used by the selected mode are converted to inputs and outputs as required. To move from the configuration state to operation, the configuration file must be loaded completely and either $\overline{\text{CON}}$ or $\overline{\text{CS}}$ must be high. During operation, the I/O pins behave according to the specified design.

Control Register

The Integrated Development System generates the bit-stream file used to configure the FPGA. In addition to the actual data to be loaded into the SRAM, the bit stream loads a control register containing eight bits used to control various configuration sequence parameters (Figure 1).

Figure 1. Control Register

B7	B6	B5	B4	B3	B2	B1	B0
----	----	----	----	----	----	----	----

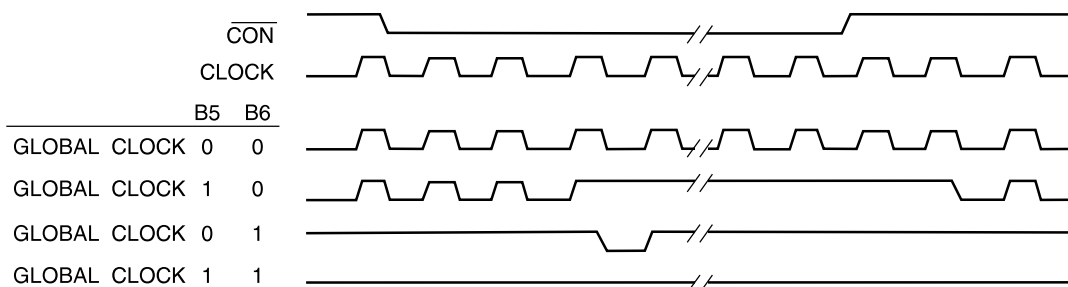
B0

B0 controls the value of the device's memory address counter after each configuration sequence. The default resets the value, so subsequent configuration sequences load the configuration file from the same address. In modes 1 and 5, the default address is 0000, in mode 2 it is 1FFFF. When B0 is set, the memory address counter retains its last value, so the user can store multiple designs sequentially in an External Memory Device.

B1

B1 controls loading of a jump address into the device's memory address counter. The default ignores any jump addresses. With B1 set, the memory address counter jumps to the specified address. Using B1, configuration files can be stored as a continuous stream or as a pointer-based list.

Figure 2. Global Clock Signal During Operation



B2

B2 controls operation of the dual-function pin $\overline{\text{CSOUT}}$. When B2 is set, this pin is disabled. This is useful when a minimum pin-count configuration is desired.

B3

B3 controls the operation of the dual-function pins $\overline{\text{ERR}}$ and $\overline{\text{CHECK}}$. When B3 is set, both pins are disabled. This is useful when a minimum pin-count configuration is desired, or when design security is a concern.

B4

B4 controls the writing of configuration data after the initialization state. When B4 is set, configuration data can not be written into the device by subsequent configuration cycles. B4 can only be reset by powering down or soft rebooting the device.

B5 and B6

B5 and B6 control the operation of the global clock signal received through the CLOCK pin.

B5	B6	Global Clock Operation
0	0	Normal operation.
1	0	Stops after third rising edge of CLOCK after $\overline{\text{CON}}$ is low. Continues after second rising edge of CLOCK after $\overline{\text{CON}}$ is high.
0	1	Stops after fourth rising edge of CLOCK after $\overline{\text{CON}}$ is high. Each configuration cycle thereafter, it receives one pulse after the third rising edge of CLOCK after $\overline{\text{CON}}$ is low.
1	1	Stops at second rising edge of CLOCK after $\overline{\text{CON}}$ is high. Remains stopped regardless of $\overline{\text{CON}}$.

Figure 2 shows the waveforms associated with each combination.

B7

B7 controls the $\overline{\text{CEN}}$ pin. When B7 is set, $\overline{\text{CEN}}$ is disabled.

Configuration State Machine

Configuration is executed by a synchronous state machine that controls the flow of configuration data into the FPGA (Figure 3). The state machine is clocked by CCLK whether the signal is externally supplied or generated internally. On each CCLK cycle a different byte or bit of the configuration file is loaded into the state machine.

Data flow is controlled by the external input signals M0, M1, M2, $\overline{\text{CON}}$, $\overline{\text{CS}}$, CHECK, D0-D7 and the values in the configuration control register. The state machine generates all the internal control signals as well as the A0-A16 output signals, $\overline{\text{ERR}}$ output, and $\overline{\text{CSOUT}}$ signal. Data is loaded into the device in a stream format and has no absolute address.

The process starts on power-up or when a mode 0 reset is applied. The reboot phase lasts for approximately 8000 up to approximately 16000 internal clock cycles while all the internal SRAM cells are written to a "0" value. During reboot the mode pins are sampled and the configuration-clock output starts.

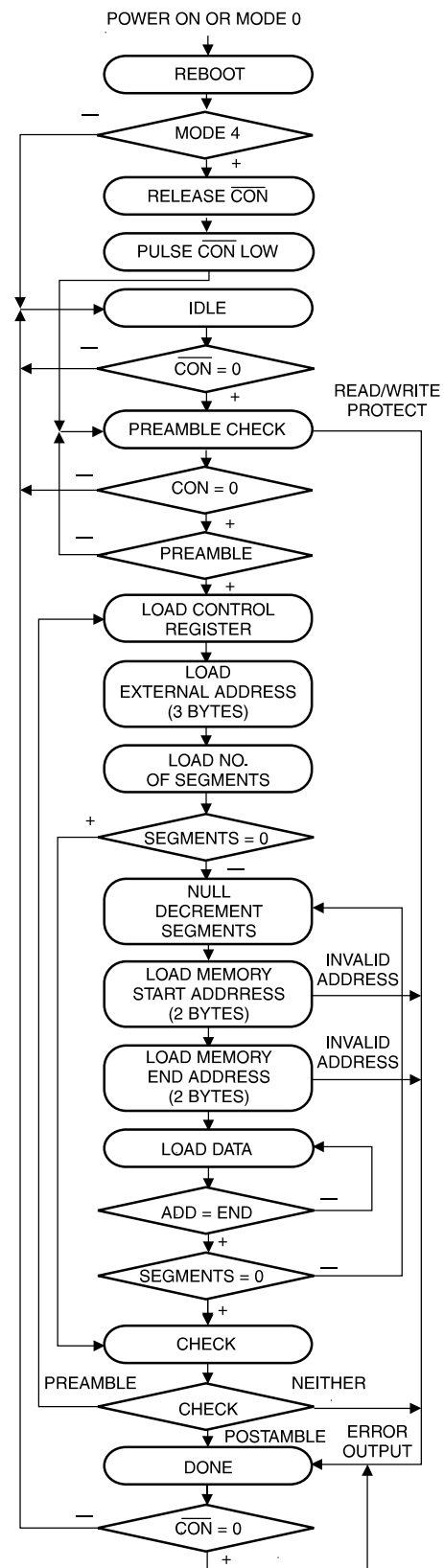
Mode 4 supports automatic configuration. During reboot, the CCLK pin is enabled for output. After reboot, mode 4 releases the $\overline{\text{CON}}$ pin, allowing it to be pulled high, and then drives it low again to begin a configuration cycle automatically.

In the modes 1, 2, 3 and 6, CCLK remains an input but is ignored until the reboot process is complete. After reboot, the other modes release $\overline{\text{CON}}$ and allow it to float high. Control of the state machine is then transferred from the internal clock to the CCLK input signal. The device remains in idle until the $\overline{\text{CON}}$ pin is driven low.

Driving $\overline{\text{CON}}$ low puts the device in the preamble check loop, a synchronizing procedure for both parallel and serial configuration modes. Configuration is dependent on the sequence of data, and the preamble specifies the first byte of the data stream. In modes 3 and 4, the preamble also defines the byte boundary of serial data, which may be parallel before being processed by the state machine. The first error test is done during the preamble check. If a read or write protect bit appears in the control register of the preamble, the $\overline{\text{ERR}}$ pin goes low and the device goes directly to the done state.

After the preamble check, the state machine loads the configuration control register and drives and holds the $\overline{\text{CON}}$ signal low until configuration is complete. Loading the configuration control register puts the next byte in the stream file into the control register, which controls features and variations in the configuration process.

Figure 3. Configuration State Machine



The state machine then loads the next three bytes into a temporary register used to parallel-load the external address counter. This action is similar to a microprocessor “jump” command. The address bytes are loaded in all modes, but the jump can only be used by modes 1, 2 and 5.

The next byte in the stream file indicates the number of data strings, or segments. A single file can have 0 to 255 segments. The byte is loaded into a counter which is decremented at the end of each data string until it reaches zero and configuration is complete.

If the register count is not zero, the state machine loads a null byte. If the B1 bit of the control register is equal to one the first time the state machine enters the null state, the external address is loaded. The byte loaded, while in the null state, is not used. If the segment count is zero, the state machine goes to the check state.

The data segment loop consists of the null byte, two bytes which load the internal pointer start address, two bytes which load the internal pointer end address, and enough data bytes to equal the difference between the end points. The state machine loops, loading data and incrementing the address counter, until the internal address pointer equals the end address pointer. Then it checks the segment counter. If more segments are to be loaded, the machine returns to the null state; and the data segment loop is executed again. If the segment counter is zero, the state machine goes to the check state. If an invalid value is encountered for the internal start or end address, the ERR signal switches low; and the state machine moves directly to the done state.

In the check state, the next byte in the stream file is examined. When a single device is being configured, this byte is a postamble, and the state machine moves to the done state. When devices are cascaded together for multiple configurations, this byte is a preamble for the next configuration file. The state machine transfers the data to the downstream device and monitors the downstream bit

stream data to determine the next check for a preamble byte. If the state machine encounters a byte that isn’t a preamble or a postamble, the ERR signal switches low; and the state machine enters the done state.

The done state releases the CON pin and loops until CON goes high and the device enters the idle state. In modes 1, 2, 5 and 6, the device enters the idle state three CCLK edges after CON is high. In modes 3 and 4, it takes twenty-four CCLK edges for the device to reach idle. The CCLK signal must therefore continue after the postamble until the device reaches the idle state.

Partial Configuration

Figure 4 gives the bit stream file used to configure a hypothetical device that has a 6 x 6 array of cells lined with four I/O on each side. Configuration begins with the bottom left cell, number 0, and ends with the upper right cell, number 35. Then the I/O cells are configured, beginning at number 36 and proceeding clockwise to number 51.

By placing windows in the bit stream file, it is possible to configure only a portion of the array. Figure 5 gives the bit stream file used to configure the lower right portion of the array and I/Os 45, 46 and 47— the program leaves darkened cells untouched.

On line six the program states that there are four segments of data to configure. The start address is the left-most cell in the bottom row to be configured, number 9, and the end address is the right-most cell in the row, number 11. Four bytes of data are used to load the cell between the two points, number 10. The next segment configures the row above. Notice that the cells between the first segment end address and the second segment start address are omitted. The data in these cells is left untouched – only the cell being programmed on a given clock cycle is changed. The other cells function as if in their normal operational mode. This means a portion of the array can be configured while the rest of the array remains operational.

Table 3. Bit-stream Sizes (bytes of data)

Mode(s)	Type ⁽¹⁾⁽²⁾	Beginning Sequence	6002	6003	6005	6010
1	P	Preamble	2677	4153	8077	16393
2	P	Preamble	2677	4153	8077	16393
3	S	Null Byte/Preamble	2678	4154	8078	16394
4	S	Null Byte/Preamble	2678	4154	8078	16394
5	P	Preamble	2677	4153	8077	16393
6	P	Preamble/Preamble	2678	4154	8078	16394

Notes: 1. P = Parallel
2. S = Serial

Figure 4. Full Configuration Example

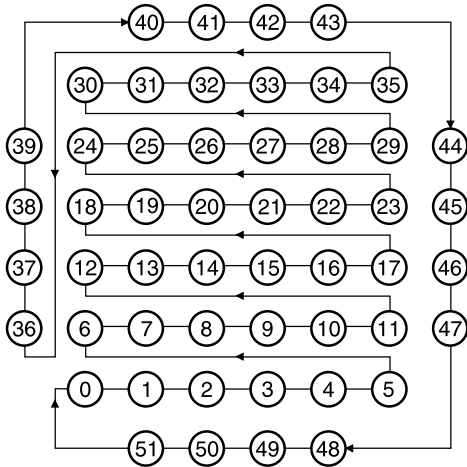
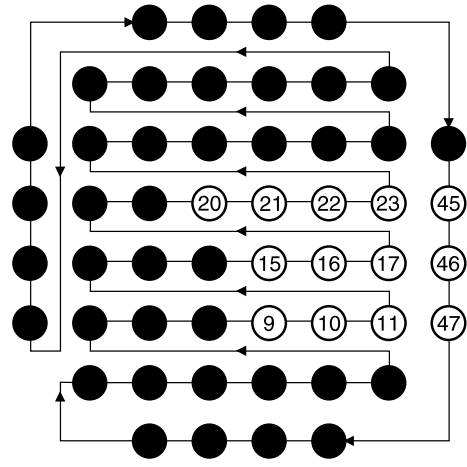


Figure 5. Partial Configuration Example



Full Configuration

```

10110010      ; preamble
00000000      ; control register
00000000      ; external address lsb
00000000      ;
00000000      ; external address msb
11111110      ; number of window segments
00000000      ; null
00000000      ; start address
00000000      ;
00000000      ; end address
00110011      ;
00000000      ; data
00000001
00000010
00000011
00000100
.
.
00110010
00110011
01001101      ; postamble
    
```

Partial Configuration

```

10110010      ; preamble
00000000      ; control register
00000000      ; external address lsb
00000000      ;
00000000      ; external address msb
11111011      ; number of window segments
00000000      ; null
00000000      ; start address segment 1
00001001      ;
00000000      ; end address
00010011      ;
00001001      ; data
00001010
00001011
00000000      ; null
00000000      ; start address segment 2
00001111      ;
00000000      ; end address
00010001      ;
00001111      ; data
00010001
00010001
.
.
00000000      ; null
00000000      ; start address segment 4
00101101      ;
00000000      ; end address
00101111      ;
00101101      ; data
00101110
00101111
01001101      ; postamble
    
```

Configuration Compression

A configuration compression algorithm, included in the Integrated Development System, uses windowing to compress the configuration file. On power-up, all cells in the FPGA are programmed to be logical zeros. Unused cells in a design remain zeros, so they do not need to be configured. The compression algorithm skips unused cells and can reduce file size by up to 80%. This in turn reduces configuration time and memory storage requirements. It even makes designs less susceptible to reverse engineering, due to the random start and end array addresses in the compressed bit stream. For more information about the configuration compression algorithm, refer to the FPGA application notes.

Configuration Modes

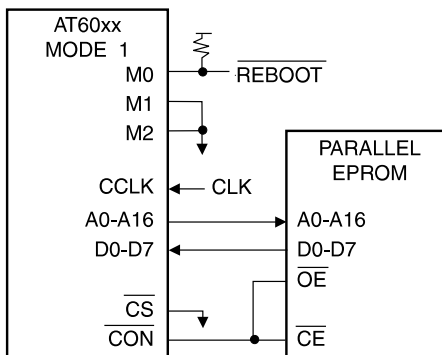
This section gives setup requirements and usage guidelines for each configuration mode.

Mode 0: Configuration Reset

Configuration Data Source	Internal
Dedicated Configuration Pins Used	$\overline{\text{CON}}$, $\overline{\text{CS}}$, M0, M1, M2, CCLK
Dual-function Pins Used	None
Optional Dual-function Pins	None

Mode 0 initiates the reboot sequence – it is equivalent to turning power to the device off and on again. Mode 0 overrides any other configuration sequences and cannot be stopped. In AT6000 devices, mode 0 is enabled by asserting $\overline{\text{CS}}$, $\overline{\text{CON}}$, M0, M1 and M2 low during the rising edge of CCLK. Reboot starts when the mode pins are released from mode 0 to any other mode. Because of this, the device should not be powered up in mode 0. One clock after entering mode 0, CSOUT tristates. Users who cascade devices and intend to use the mode 0 reboot function should insert logic to guarantee that the $\overline{\text{CS}}$ signal sent to the downstream cascaded device is driven low.

Figure 6. Mode 1 Configuration



Mode 1: Address Count-up, External CCLK

Configuration Data Source	Parallel EPROM
Dedicated Configuration Pins Used	$\overline{\text{CON}}$, $\overline{\text{CS}}$, M0, M1, M2, CCLK
Dual-function Pins Used	D0-D7, A0-A16
Optional Dual-function Pins	$\overline{\text{ERR}}$, $\overline{\text{CHECK}}$, $\overline{\text{CSOUT}}$, $\overline{\text{CEN}}$

Mode 1 (Figure 6) does not automatically generate a $\overline{\text{CON}}$ signal after the power-up boot sequence. The user supplies a configuration clock to CCLK. Configuration is initiated by driving $\overline{\text{CON}}$ low.

If the FPGA is sharing a large EPROM with a microprocessor, the addresses used must start from the opposite end of the EPROM address map so that configuration does not interfere with the microprocessor, and vice versa. In mode 1, the external address counter starts at 00000 and counts up (see mode 2 description).

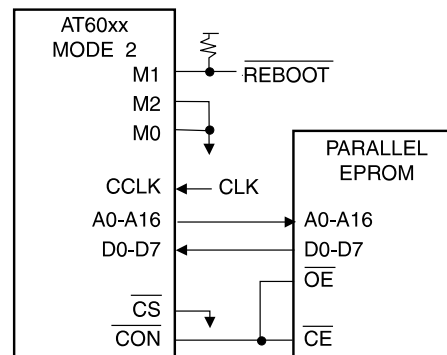
Using a maximum clock rate of 10 MHz, mode 1 can configure a single device in under 1 millisecond. Cascading devices limits the parallel data rate to 800 kHz.

Mode 2: Address Count-down, External CCLK

Configuration Data Source	Parallel EPROM
Dedicated Configuration Pins Used	$\overline{\text{CON}}$, $\overline{\text{CS}}$, M0, M1, M2, CCLK
Dual-function Pins Used	D0-D7, A0-A16
Optional Dual-function Pins	$\overline{\text{ERR}}$, $\overline{\text{CHECK}}$, $\overline{\text{CSOUT}}$, $\overline{\text{CEN}}$

Mode 2 (Figure 7) does not automatically generate a $\overline{\text{CON}}$ signal after the power-up boot sequence. The user supplies a configuration clock to CCLK. Configuration is initiated by driving $\overline{\text{CON}}$ low.

Figure 7. Mode 2 Configuration



A typical microprocessor uses the highest or lowest address to load its own reboot address vector. If the FPGA is sharing a large EPROM with a microprocessor, the addresses used must start from the opposite end of the EPROM address map so that configuration does not interfere with the microprocessor, and vice versa. In mode 2, the external address counter starts at 1FFFF and counts down (see mode 1 description).

Using a maximum clock rate of 10 MHz, mode 2 can configure a single device in under one millisecond. Cascading devices limits the parallel data rate to 1 MHz.

Mode 3: Bit-sequential, External CCLK

Configuration Data Source	Serial EPROM, Serial Comm. Port, UART, Download Cable
Dedicated Configuration Pins Used	CON, CS, M0, M1, M2, CCLK
Dual-function Pins Used	D0
Optional Dual-function Pins	ERR, CHECK, CSOUT

Mode 3 (Figure 8) does not automatically generate a $\overline{\text{CON}}$ signal after the power-up boot sequence. The user must supply a configuration clock to CCLK. Configuration is initiated by driving $\overline{\text{CON}}$ low.

As long as data setup and hold requirements are satisfied, CCLK pulses can have arbitrary periods. This is helpful when using asynchronous communication ports or UARTs for configuration. If CCLK is stopped entirely between configurations, allow 24 preceding and trailing clock pulses

with respect to $\overline{\text{CON}}$ going low or high (refer to the AC timing table in the AT6000 Series data sheet).

Depending on the speed of the user-supplied clock, mode 3 configuration can take as little as 8 milliseconds.

Mode 3 can be used to configure multiple devices cascaded together (Figure 9). The first device in the cascade chain must use either mode 3 or mode 4. If the configuration file contains a second preamble instead of a postamble (see the configuration-file format section), then the first device in the chain drives $\overline{\text{CSOUT}}$ low enabling the next device in the chain to receive configuration data from the serial data source. Configuration for downstream devices proceeds in a similar manner with "chip select" ($\overline{\text{CS}}$) propagating through the chain.

Figure 8. Mode 3 Configuration

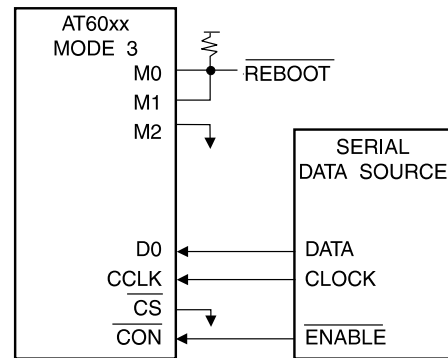
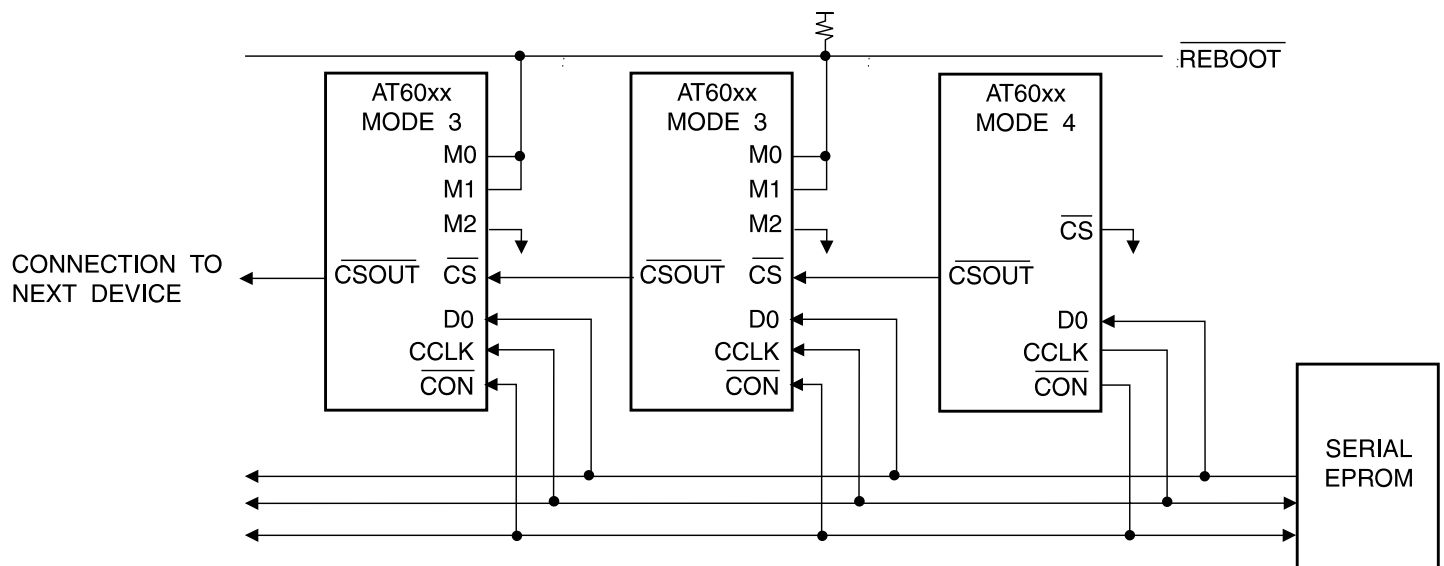


Figure 9. Mode 3 Cascade



Mode 3 is used when configuring with the download cable provided in the Integrated Development System.

Mode 4: Bit-sequential, Internal CCLK EEPROM (AT17XXX)

Configuration Data Source	Serial EEPROM
Dedicated Configuration Pins Used	$\overline{\text{CON}}$, $\overline{\text{CS}}$, M0, M1, M2, CCLK
Dual-function Pins Used	D0
Optional Dual-function Pins	$\overline{\text{ERR}}$, $\overline{\text{CHECK}}$, $\overline{\text{CSOUT}}$

Mode 4 (Figure 10) asserts the $\overline{\text{CON}}$ pin low during the power-up boot sequence. $\overline{\text{CON}}$ is released for one CCLK period after initialization to reset the serial EEPROM. $\overline{\text{CON}}$ is then automatically re-asserted low and an internal oscillator toggles CCLK. This causes the EEPROM to begin downloading configuration data. One bit of data is loaded from the D0 pin on each rising edge of CCLK until configuration is complete. $\overline{\text{CON}}$ is then released, indicating the device is ready to use. Configuration time varies depending on the speed of the internal oscillator, but typically takes about 8 milliseconds.

The power supply ramp-up rate is critical in mode 4. The device generates a reset pulse 8 milliseconds after the supply voltage crosses the V_{TRIP} level (Figure 11). The supply voltage must be at the minimum for the serial EEPROM before the FPGA generates its reset pulse. Otherwise, the EEPROM's operation may be sporadic.

Figure 10. Mode 4 Configuration

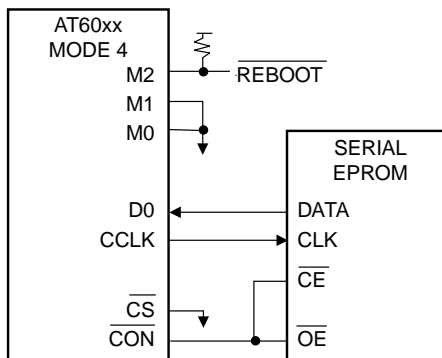
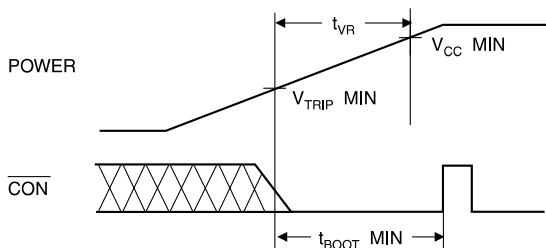


Figure 11. Power Supply Ramp-up (Mode 4)



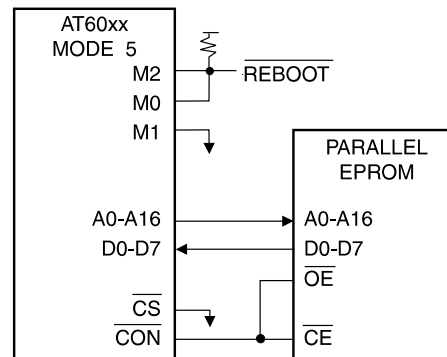
Mode 5: Address Count-up, Internal CCLK

Configuration Data Source	Parallel EPROM
Dedicated Configuration Pins Used	$\overline{\text{CON}}$, $\overline{\text{CS}}$, M0, M1, M2, CCLK
Dual-function Pins Used	D0-D7, A0-A16
Optional Dual-function Pins	$\overline{\text{ERR}}$, $\overline{\text{CHECK}}$, $\overline{\text{CSOUT}}$, $\overline{\text{CEN}}$

Mode 5 (Figure 12) does not automatically generate a $\overline{\text{CON}}$ signal after the power-up boot sequence. Configuration is initiated by driving $\overline{\text{CON}}$ low. An internal oscillator toggles CCLK. This causes the FPGA to generate addresses A0-A16, beginning at 0, to read a configuration file from a parallel EPROM. One byte of configuration data is loaded from the D0-D7 pins on each rising edge of CCLK until configuration is complete. $\overline{\text{CON}}$ is then released, indicating the device is ready to use. Configuration time varies depending on the speed of the oscillator, but typically takes 8 milliseconds for the AT6005, and 16 milliseconds for the AT6002/3/10.

Only 13 address bits are required to fully program a single device; the four extra addresses allow multiple device configuration and let the device share memory space with other components of a system.

Figure 12. Mode 5 Configuration



$V_{\text{CC min}}$	Minimum voltage for EEPROM operation
$V_{\text{TRIP min}}$	Minimum FPGA supply voltage to initiate reboot
$t_{\text{BOOT min}}$	Minimum reboot cycle time
t_{VR}	Minimum rise time of power supply from V_{TRIP} to $V_{\text{CC min}}$

Mode 6: Byte-sequential, External CCLK

Configuration Data Source	Parallel port of microprocessor
Dedicated Configuration Pins Used	$\overline{\text{CON}}$, $\overline{\text{CS}}$, M0, M1, M2, CCLK
Dual-function Pins Used	D0-D7
Optional Dual-function Pins	$\overline{\text{ERR}}$, $\overline{\text{CHECK}}$, $\overline{\text{CSOUT}}$

Mode 6 (Figure 13) loads data in 8-bit words to decrease configuration time. It does not use the address pins; each byte in the data stream is setup and held with respect to the rising edge of CCLK.

Mode 6 may be used in a configuration chain (Figure 14) or with the parallel port of a microprocessor or system bus, and may be best for a “smart system” in which the user intends to reconfigure the FPGA as a regular part of system operation. More than one device can be configured by tying all the data buses together and connecting the $\overline{\text{CON}}$ pins. The $\overline{\text{CS}}$ pin can then be used to select individual devices for configuration (Figure 15).

Figure 13. Mode 6 Configuration

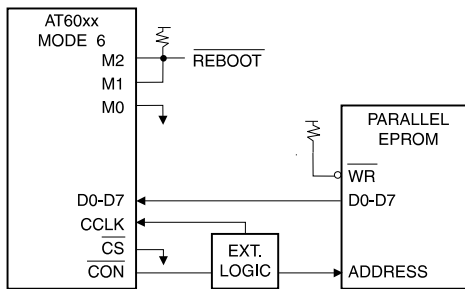


Figure 14. Mode 6 Cascade

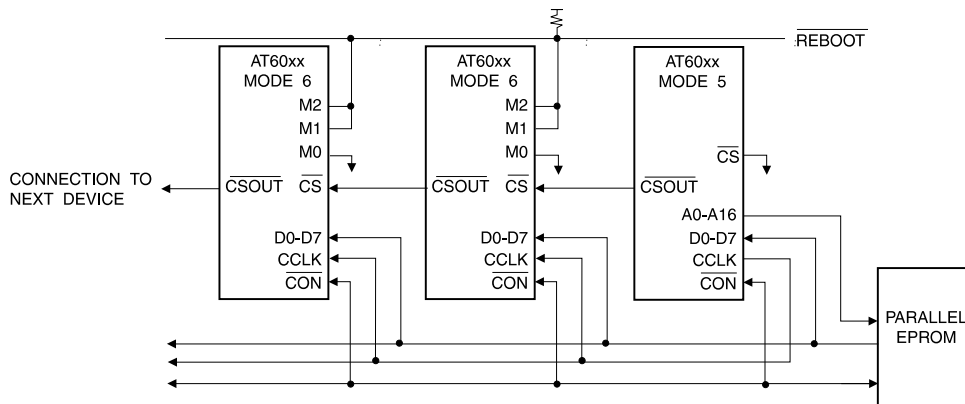
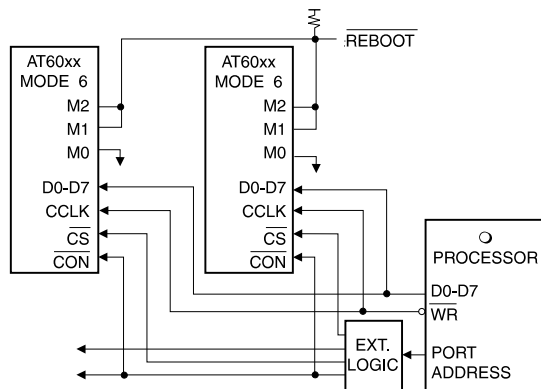


Figure 15. Parallel Configuration with Mode 6



Configuration Timing Parameters - 5V

These parameters are based on the timing diagrams that follow.

Parameter	Description	Min	Typ	Max	Units	
t_{BOOT}	Delay from release of mode 0 or Power on ($V_{CC} > V_{sth}$ min) to \overline{CON} released.	AT6002/3: modes 1,2,3,5,6	1.3	2.7	5.4	ms
		AT6002/3/10: mode 4	8.1	16.3	32.6	ms
		AT6005: modes 1,2,3,4,5,6	4.4	8.8	17.6	ms
		AT6010: modes 1,2,3,5,6	0.05	0.1	0.2	ms
t_{WCON}	\overline{CON} and \overline{CS} high pulse width. Measured in CCLK clock cycles in modes 1, 2, 3 and 6.	2			cyc	
t_{PCON}	\overline{CON} high pulse width. Measured in CCLK clock cycles in modes 4 and 5.	2		2	cyc	
t_{PUZ}	Delay from power-up or entry into mode 0 to user I/Os being tri-stated.		2000	4000	ns	
t_{DERR}	Delay time from CCLK to change in \overline{ERR} . \overline{ERR} will typically be high, and only go low if there is an error during configuration or a mismatch during the check function.			30	ns	
t_{SM}	Setup time from M0, M1, M2, \overline{CS} and \overline{CON} to rising edge of CCLK to initiate configuration or reboot.	30			ns	
t_{HMP}	Hold time for \overline{CS} and \overline{CON} from rising edge of CCLK with preamble data present. Valid in modes 1, 2, 5 and 6.	2			cyc	
t_{HMS}	Hold time for \overline{CS} and \overline{CON} from rising edge of CCLK with the least-significant-bit of the preamble present. Valid in modes 3 and 4.	17			cyc	
t_{HCD}	Hold time for configuration data with respect to rising edge of CCLK.	5			ns	
t_{SCD}	Setup time for configuration data with respect to rising edge of CCLK.	10			ns	
t_{CFG}	Delay from rising edge of CCLK to change in I/O pin direction, as required when moving between the configuration and operation states.			50	ns	
t_{DA}	Delay from CCLK rising edge to external address change.			35	ns	
t_{CONH}	Delay from rising edge of CCLK to \overline{CON} release. Delay measured with 2.7k pull-up resistor on \overline{CON} .			35	ns	
t_{SC}	Setup time for M0, M1, M2 and CCLK to \overline{CON} high.	10			cyc	
V_{TRIP}	Supply voltage at which FPGA initiates reboot.	2.8		4.75	V	
t_{CS}	Delay time from falling edge of CCLK to change in \overline{CSOUT} .			30	ns	

Table 4. CCLK Parameters - 5V

Mode(s)	Condition	t_{CCLKL}	t_{CCLKH}	t_{PCCLK}		
		Min	Min	Min	Typ	Max
1, 2, 6	Without Cascade, without \overline{CHECK}	40 ns	40 ns	80 ns		
1, 2, 6	With Cascade, without \overline{CHECK}	40 ns	40 ns	80 ns		
1, 2, 6	Without Cascade, with \overline{CHECK}	200 ns	200 ns	500 ns		
1, 2, 6	With Cascade, with \overline{CHECK}	200 ns	200 ns	1.0 μ s		
4, 5	CCLK is Output	240 ns	240 ns	600 ns	1000 ns	1600 ns
3	Without \overline{CHECK}	40 ns	40 ns	80 ns		
3	With \overline{CHECK}	200 ns	200 ns	500 ns		

Configuration Timing Parameters - 3.3V

These AC parameters are based on the timing diagrams that follow.

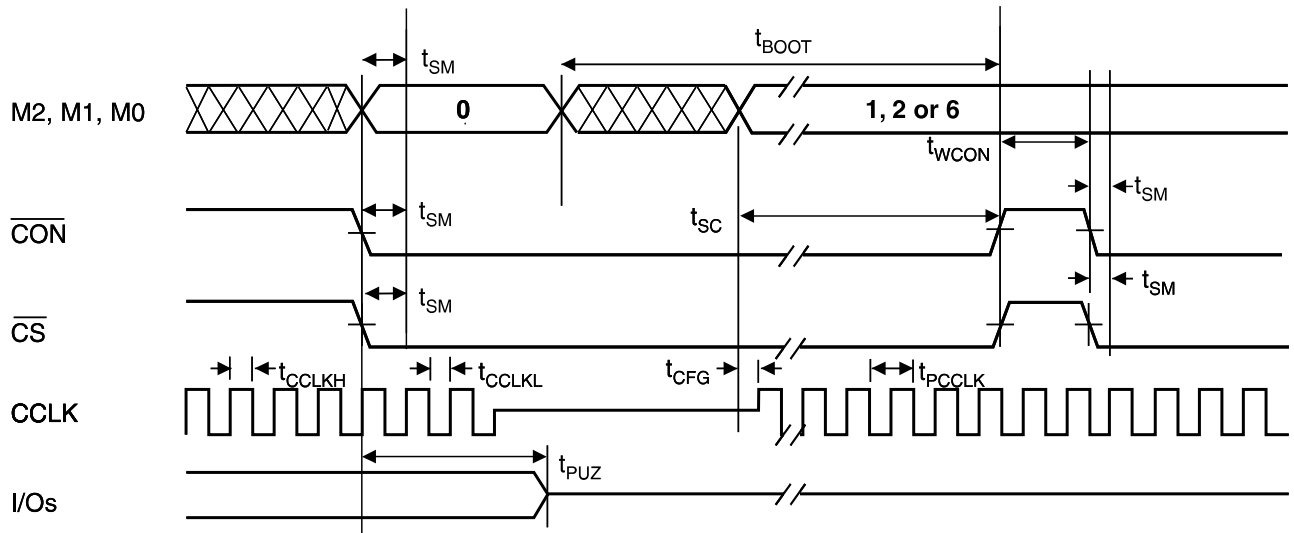
Parameter	Description	Min	Typ	Max	Units	
t_{BOOT}	Delay from release of mode 0 or Power on ($V_{CC} > V_{sth}$ min) to \overline{CON} released.	AT6002/3: modes 1,2,3,5,6	2.6	5.4	10.8	ms
		AT6002/3/10: mode 4	16.2	32.6	65.2	ms
		AT6005: modes 1,2,3,4,5,6	8.8	17.6	35.2	ms
		AT6010: modes 1,2,3,5,6	0.10	0.2	0.4	ms
t_{WCON}	\overline{CON} and \overline{CS} high pulse width. Measured in CCLK clock cycles in modes 1, 2, 3 and 6.	2			cyc	
t_{PCON}	\overline{CON} high pulse width. Measured in CCLK clock cycles in modes 4 and 5.	2		2	cyc	
t_{PUZ}	Delay from power-up or entry into mode 0 to user I/Os being tri-stated.		4000	8000	ns	
t_{DERR}	Delay time from CCLK to change in \overline{ERR} . \overline{ERR} will typically be high, and only go low if there is an error during configuration or a mismatch during the check function.			60	ns	
t_{SM}	Setup time from M0, M1, M2, \overline{CS} and \overline{CON} to rising edge of CCLK to initiate configuration or reboot.	60			ns	
t_{HMP}	Hold time for \overline{CS} and \overline{CON} from rising edge of CCLK with preamble data present. Valid in modes 1, 2, 5 and 6.	2			cyc	
t_{HMS}	Hold time for \overline{CS} and \overline{CON} from rising edge of CCLK with the least-significant-bit of the preamble present. Valid in modes 3 and 4.	17			cyc	
t_{HCD}	Hold time for configuration data with respect to rising edge of CCLK.	10			ns	
t_{SCD}	Setup time for configuration data with respect to rising edge of CCLK.	20			ns	
t_{CFG}	Delay from rising edge of CCLK to change in I/O pin direction, as required when moving between the configuration and operation states.			100	ns	
t_{DA}	Delay from CCLK rising edge to external address change.			70	ns	
t_{CONH}	Delay from rising edge of CCLK to \overline{CON} release. Delay measured with 2.7 k pull-up resistor on \overline{CON} .			70	ns	
t_{SC}	Setup time for M0, M1, M2 and CCLK to \overline{CON} high.	10			cyc	
V_{TRIP}	Supply voltage at which FPGA initiates reboot.	2.8		3.0	V	
t_{CS}	Delay time from falling edge of CCLK to change in \overline{CSOUT} .			60	ns	

Table 5. CCLK Parameters - 3.3V

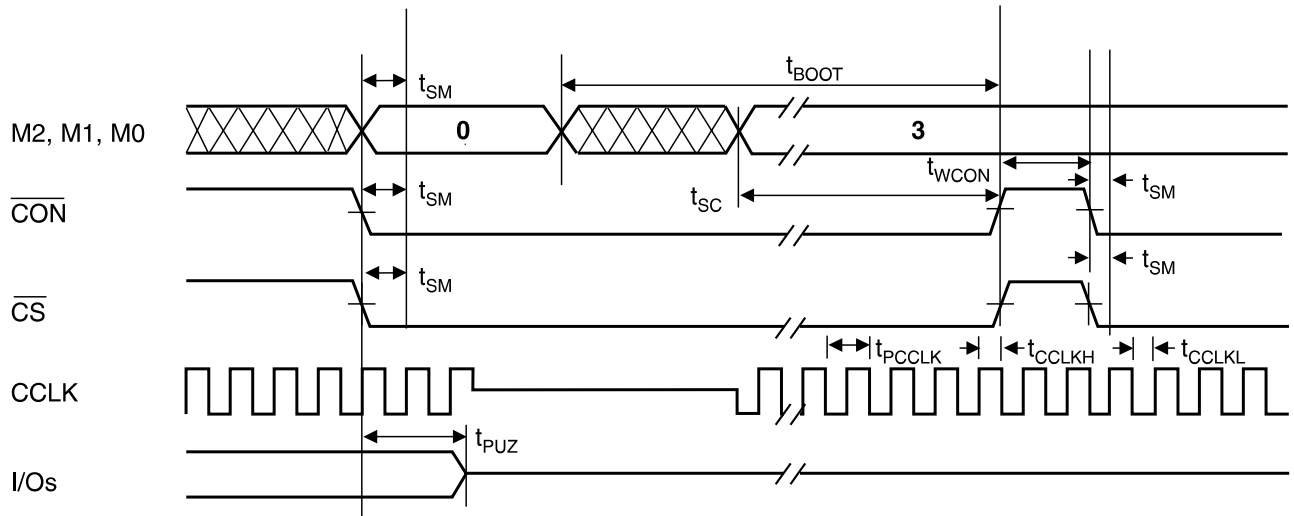
Mode(s)	Condition	t _{CCLKL}	t _{CCLKH}	t _{PCCLK}		
		Min	Min	Min	Typ	Max
1, 2, 6	Without Cascade, without $\overline{\text{CHECK}}$	80 ns	80 ns	160 ns	2000 ns	3200 ns
1, 2, 6	With Cascade, without $\overline{\text{CHECK}}$	80 ns	80 ns	160 ns		
1, 2, 6	Without Cascade, with $\overline{\text{CHECK}}$	400 ns	400 ns	1 μ s		
1, 2, 6	With Cascade, with $\overline{\text{CHECK}}$	400 ns	400 ns	2.0 μ s		
4, 5	CCLK is Output	480 ns	480 ns	1000 ns		
3	Without $\overline{\text{CHECK}}$	80 ns	80 ns	160 ns		
3	With $\overline{\text{CHECK}}$	400 ns	400 ns	1 μ s		

Reboot Cycle

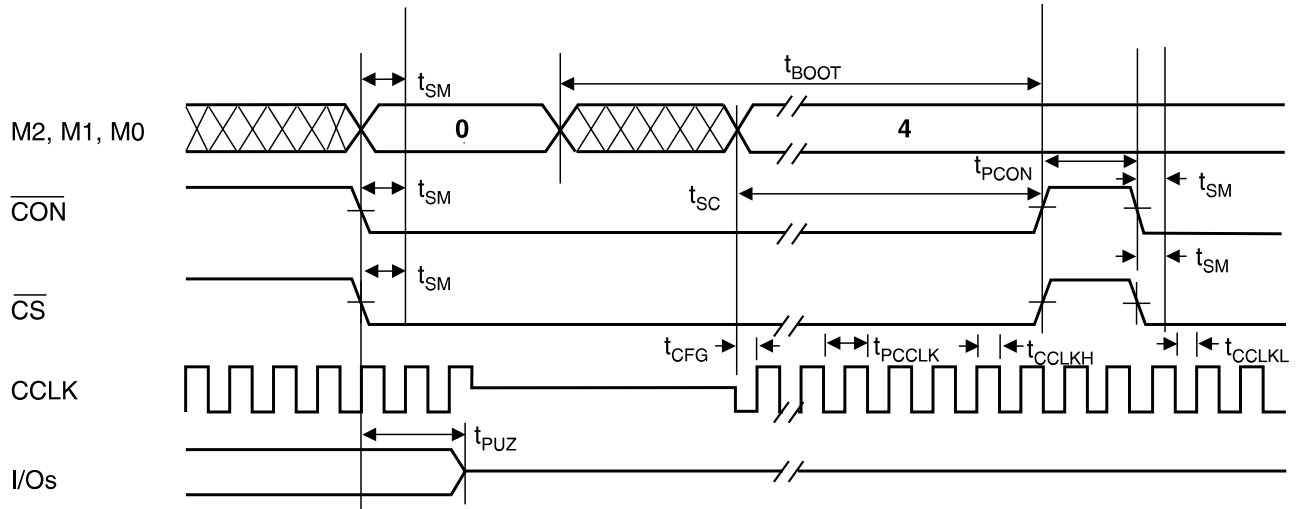
Modes 1, 2, and 6



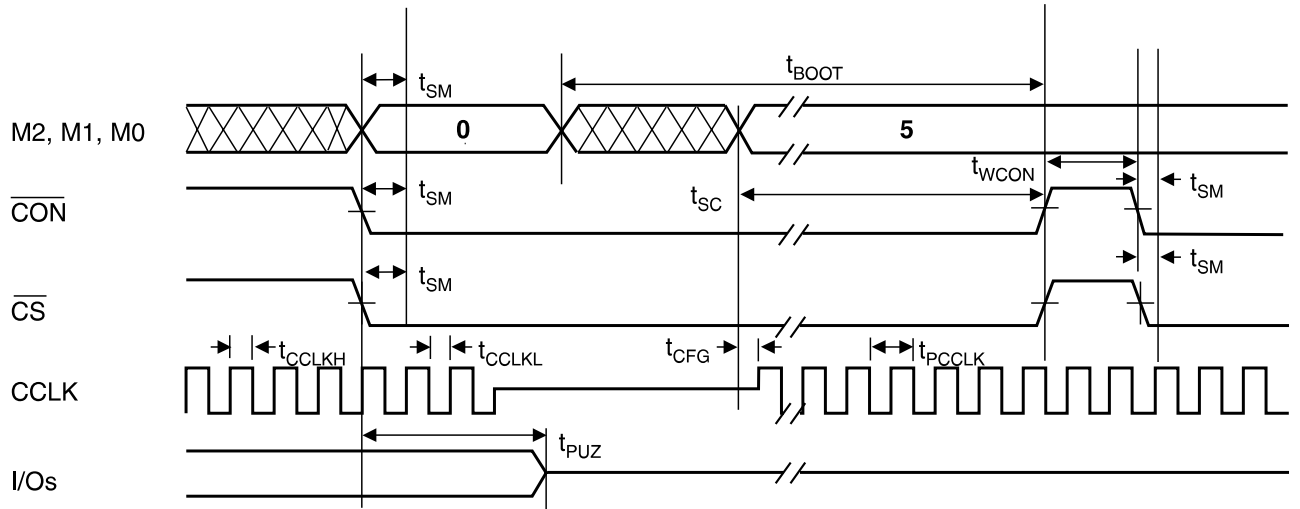
Mode 3



Mode 4

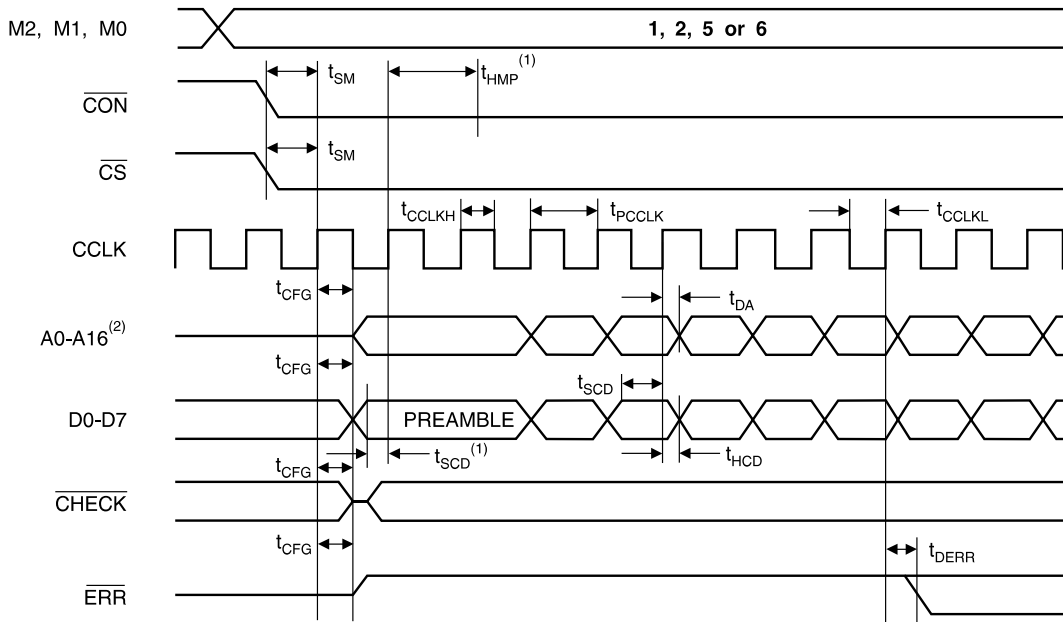


Mode 5



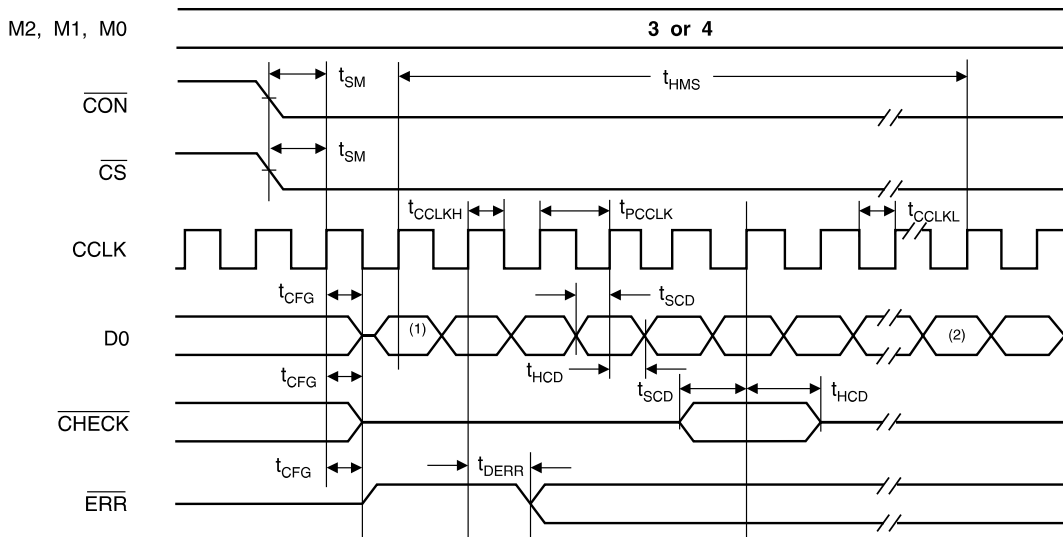
Beginning of Configuration

Modes 1, 2, 5, and 6



- Notes:
1. Measured with respect to the edge of CCLK, which clocks in the preamble.
 2. A0-A16 not used in mode 6.

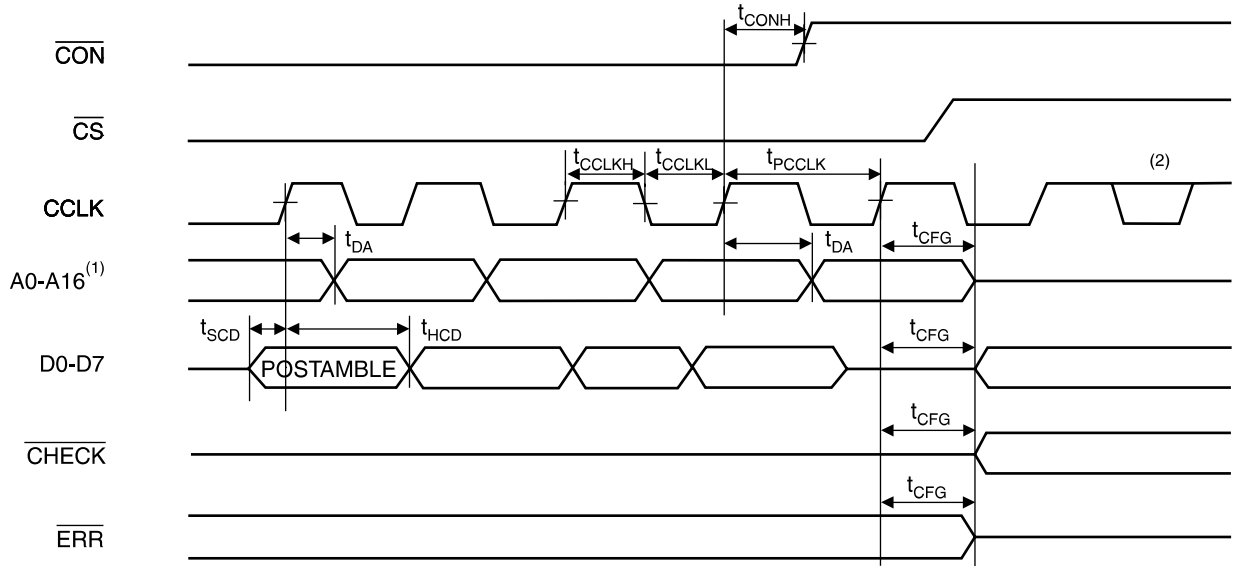
Modes 3 and 4



- Notes:
1. Preamble LSB.
 2. Preamble MSB.

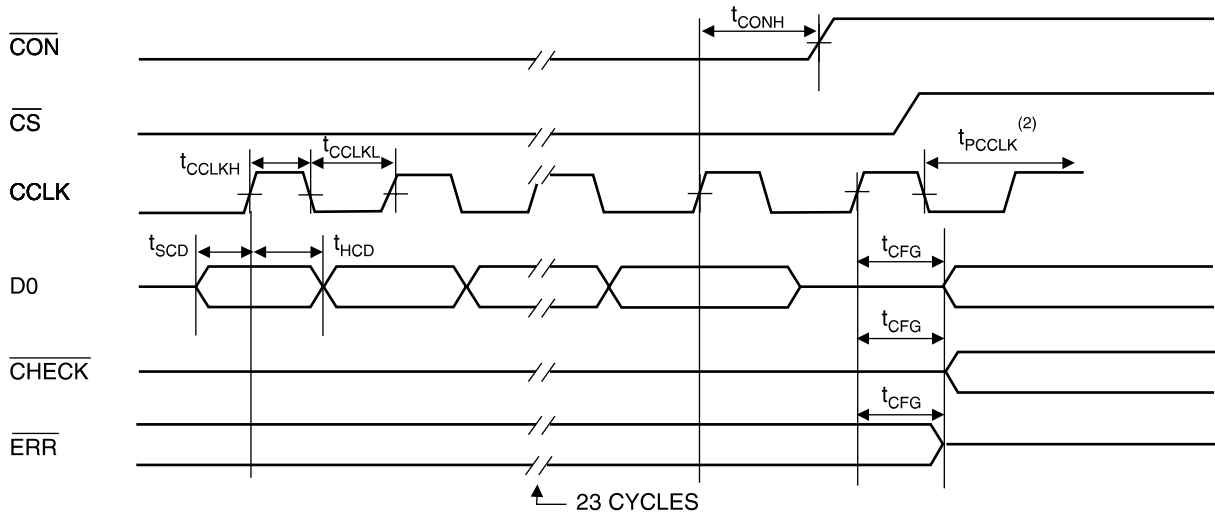
End of Configuration without Cascading

Modes 1, 2, 5, and 6



- Note: 1. A0-A16 not used in mode 6.
2. CCLK remains high in mode 5.

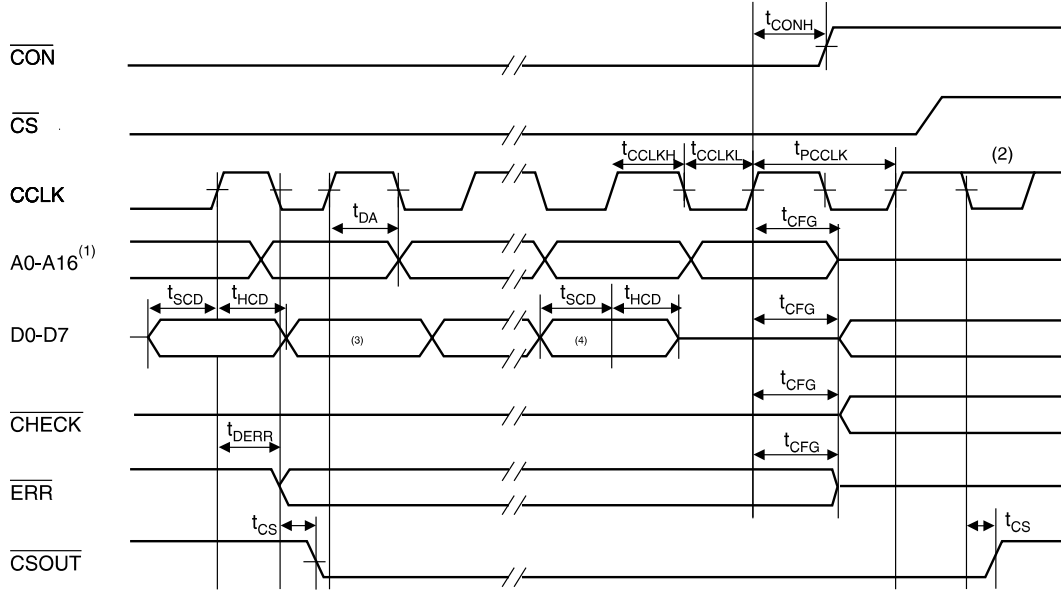
Modes 3 and 4



- Notes: 1. Postamble LSB.
2. CCLK remains high in mode 4.

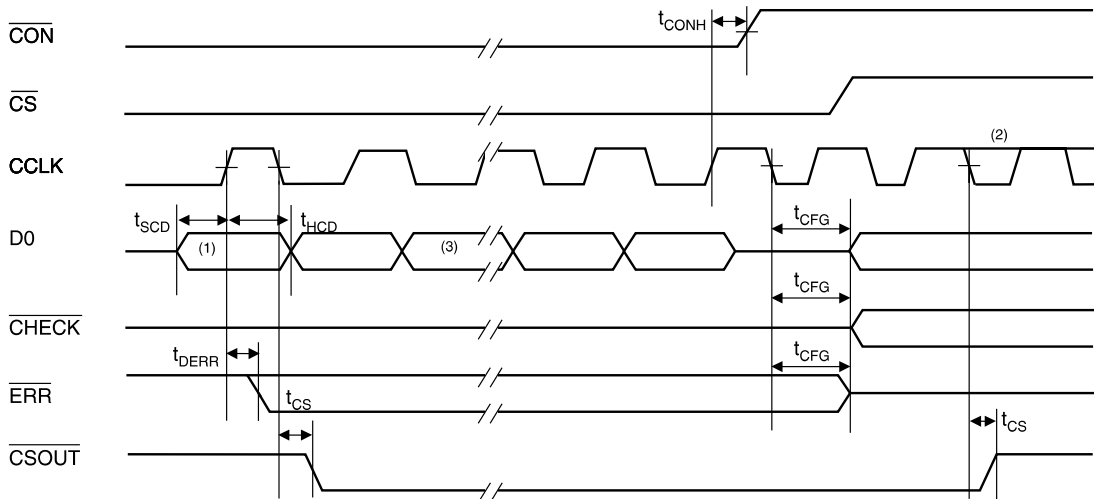
End of Configuration with Cascading

Modes 1, 2, 5, and 6



- Notes:
1. A0-A16 not used in mode 6.
 2. CCLK remains high in mode 5.
 3. End address of final window.
 4. Postamble of final chip in cascade chain.

Modes 3 and 4



- Notes:
1. Preamble LSB.
 2. CCLK remains high in mode 4.
 3. Postamble of final chip in cascade chain.



Atmel Headquarters

Corporate Headquarters

2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe

Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia

Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan

Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs

1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset

Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand

North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

BBS

1-(408) 436-4309

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