





## 2.1 MSC0407 Features

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### General

- HCMOS technology — fully static operation
- Full use of the industry-standard M68HC05 instruction set, including: 8 x 8 bits unsigned multiply instruction, true bit manipulation, memory-mapped I/O
- Advanced physical security, including removal of test mode when testing is complete
- Operating voltage: 3.0V  $\pm$  10% and 5.0V  $\pm$  10%
- Meets GSM 11.11 & 11.12 specifications
- 5.0 MHz maximum internal bus frequency at 5.0 V.
- 2.0 MHz maximum internal bus frequency at 3.0 V.
- ESD protection to  $\pm$ 4000 V
- Bond pad layout conforming to ISO standard ISO 7816/2
- External maskable interrupt on ISO standard I/O port (PA0)
- Power saving WAIT and very low power STOP modes
- Power-up detection
- Watchdog capability under software control (mask option)

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### EEPROM

- 4064 bytes of on-chip user EEPROM, plus 32 bytes that are protected in user mode
- EEPROM: 2ms programming; 10 years data retention; and typically more than 2,000,000 write/erase cycles
- On-chip charge pump for EEPROM programming, driven by an independent internal oscillator

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### RAM and ROM

- 23032 bytes of on-chip user ROM, plus eight bytes reserved for vectors
- 384 bytes of on-chip RAM

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### Peripherals

- Random number generator
- One bidirectional I/O line (1-bit ISO 7816/3 standard I/O port)
- Time base circuitry with maskable interrupt capability, built around either a free-running oscillator or an external clock source (software selectable)

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**Security**

- RAM cleared on reset (mask option)
- Accumulator and Index register cleared on reset
- Low voltage, high voltage and low frequency detection circuitry; high frequency filter on clock
- Access control logic, including read inhibit facility on selected areas of ROM or EEPROM
- Parity bit (allows the parity of the contents of any legal address to be determined)
- Illegal address reset

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**Customer options**

- Clock division ratio
- Status of COP watchdog after reset
- EEPROM control bytes read-only
- EEPROM addresses affected by lockout
- ROM addresses affected by lockout
- RAM cleared on reset
- EEPROM scrambling
- Operating voltage