



Single Quadrant and Four Quadrant Multiplier Utilising TRAC

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The TRAC family of Totally Reconfigurable Field Programmable Analog Devices offer an integrated path from signal processing problems to working silicon solutions - in minutes!

Introducing a Top-Down, Structured design discipline, TRAC enables rapid implementation, prototyping and product release. Rather than designing at the component level, TRAC champions a Computational Approach. Using eight simple mathematical building-blocks, any transfer function or mathematical equation can be implemented on TRAC, and more besides!

With a combination of programmable silicon and design software, TRAC brings a truly Integrated Route to signal processing problem solving, providing designers with benefits formerly associated only with programmable digital devices, and offering a path to Custom Silicon for higher volume users.

Introduction

The whole notion of processing analog signals by computation as opposed to the traditional methods of moulding a circuit design based upon the characteristics of components does, of course, assume that the required

system behaviour can be expressed at the top level of abstraction, entirely mathematically.

Designing mathematically does require hardware which is capable of executing a set of mathematical operations. The content of this set can be debated ad infinitum, and at present has been designed in such a way that, any mathematical equation relating to an analog function may be expressed easily. These operations are outlined as follows:

- ADD
- NEGATE
- LOG
- ANTI-LOG (ANT)
- AUX (Amplify, Differentiate, Integrate)
- REC (Rectify)

Theory of Application

One of the most common mathematical operations in signal processing is multiplication. The relative ease with which this function can be performed algorithmically in digital technology has long provided a significant edge over analog technology. While there are traditional analog circuit techniques which provide high performance multipliers, they are not easy to include in an overall ASP (Analog Signal



Processing) toolkit since they rely very much upon component-level behaviour (such as the variation of transistor transconductance with operating current). Other techniques such as Pulse Width Modulation (PWM), though performing well as an individual multiplying function, do not fit well into overall analog design strategy.

It is for these reasons that the logarithmic function was adopted. Representing numbers by their logarithms brings much greater potency to the computational problem. The multiplication of two numbers is reduced to a simple addition of their logarithms, division becomes subtraction, and raising to a power can be achieved simply by multiplying the logarithm by the required exponent.

Practical exploitation of these ideas would not be possible were it not for the remarkable consistency of the equation relating the current flowing through a silicon junction as a function of applied voltage. In approximate form it is:

$$I = I_0 (\exp(qv/kT) - 1) \quad (1)$$

where

I = current
 I_0 = junction saturation current
 q = charge on the electron
 k = Boltzmann's constant
 T = absolute temperature
 v = voltage

For all practical levels of signal this equation can be approximated as

$$I = I_0 \exp (qv/kT) \quad (2)$$

In terms of voltage, equation (2) can be

rearranged to

$$v = kT/q \log_e \left(\frac{I}{I_0} \right) \quad (3)$$

Equations (3) and (2) are the key to the generation of log and antilog operation.

Temperature Consideration

Use of the basic diode equation for the logarithmic and antilogarithmic functions does involve understanding and controlling temperature variations. First, the kT/q term of equation (1) does not pose any real problem due to the essentially complementary nature of the logarithmic and antilogarithmic operations; i.e., the term is introduced when Logs are taken early in the computation and is taken out at the end of the computation when antilogs are taken. There is a much more complex problem associated with the temperature dependence of the saturation current I_0 . While the antilog operation introduces an I_0 term (equation (2)) similar to the complementary kT/q term, the exponent of I_0 is likely to have changed in the computational procedure since it is under the Log term (equation (3)). In many cases if the value of the exponent is tracked, which is a simple matter in automated design procedures, then it may be possible to obtain compensation in a simple manner at the antilog operation. In many situations, for example, when operands are raised to arbitrary power, this will not be the case. In this situation it is advisable to remove the I_0 term at the beginning of the computation and re-introduce it at the end to compensate for that introduced by the antilog operation.

Scaling (E_{ref})

A further practical problem is scaling. In the description of ASP procedure so far, the notion of adding logarithms for multiplication has been outlined without consideration of the actual magnitude of the signals involved. The typical voltage dropped across a PN junction is around 0.6V, and the rate of change of current with voltage is around one decade for every 60mV. Hence a current range of 10,000 to 1 would require a voltage range of say only 540 to 780mV, which is quite a small change. In short, it is not just a simple matter of adding the voltages across two PN junctions since this would result in currents of staggering proportions. If, for example, a current of 1uA required a voltage of 600mV and two such voltages were added, the resultant current would be 10,000A !. The solution to this

problem is scaling, which consists of subtracting a portion of voltage (E_{ref}) in a temperature controlled manner from the logarithmic form of the signal representation. It is often convenient to combine the operations of I_0 temperature compensation and scaling.

An example of where this approach has been adopted is shown in Figure 1. It can be seen that a reference signal E_{ref} has been introduced which provides both I_0 temperature compensation and scaling.

If $E_{ref} = 1V$, mathematically, the output is seen to be the exact product of the input signals (E_a , E_b), and in addition is completely independent of temperature.

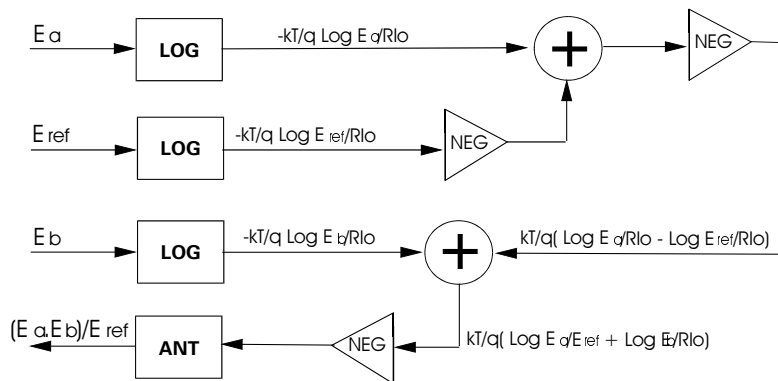


Figure 1
Single Quadrant DC Multiplier (SQM) Algorithm

Four Quadrant Multiplication

Whilst the single quadrant multiplier will provide excellent temperature independent multiplication for inputs of the positive polarity, it is often required to operate in 2,3 and 4 quadrants.

The required functionality is depicted in the block diagram shown in Figure 2.

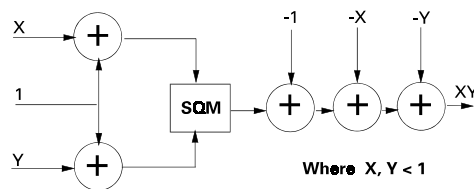


Figure 2
Four Quadrant Multiplier (4QM)

The multiplier and multiplicand, X and Y, can assume positive or negative polarity. The single quadrant multiplier will provide the core for the four quadrant multiplication which means that it must be provided with first quadrant operands. This can be achieved by biasing (adding a constant DC voltage) the inputs so that they are always of positive polarity.

The inputs to the single quadrant multiplier then become:

$$1+X \text{ and } 1+Y \text{ where } X, Y < 1$$

$$(1 + X) (1 + Y) = 1 + Y + X + XY$$

It can be seen from the result of multiplication, that the required XY product is generated but in addition the spurious terms X, Y and 1 have also been created. At this point it is relatively a simple matter of using the ADD operation to remove these extra terms.

Software

Adopting the "computational approach", TRAC multipliers add the logarithms of the multiplier and multiplicand inputs (V1 and V2). Scaling and temperature compensation is achieved by employing a reference voltage, V_{ref} (E_{ref}) as outlined by the algorithm in the previous section.

TRAC design shown in Figure 3 outlines the simplicity of transferring a mathematical algorithm and/or equation into the device and evaluating the design directly on silicon.

As it can be seen by the TRAC designs shown in Figure 3 and Figure 4, unlike the conventional multipliers, TRAC offers a single chip solution with no external components.

By adopting a scaling voltage (V_{ref}) of 1V, the output is the exact product of the inputs as demonstrated by the TRAC Multiplier algorithm.

The multiplier designs shown here, outline the benefits of TRAC as an Analog Signal Processor (ASP).

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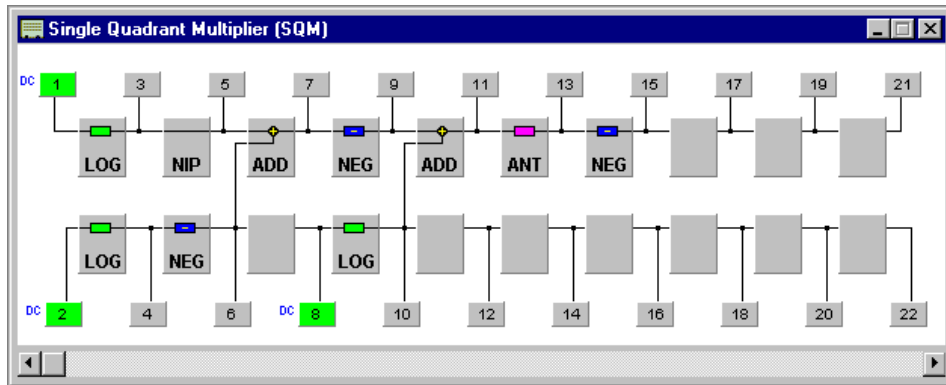


Figure 3
TRAC configured as a DC Single Quadrant Multiplier (SQM)

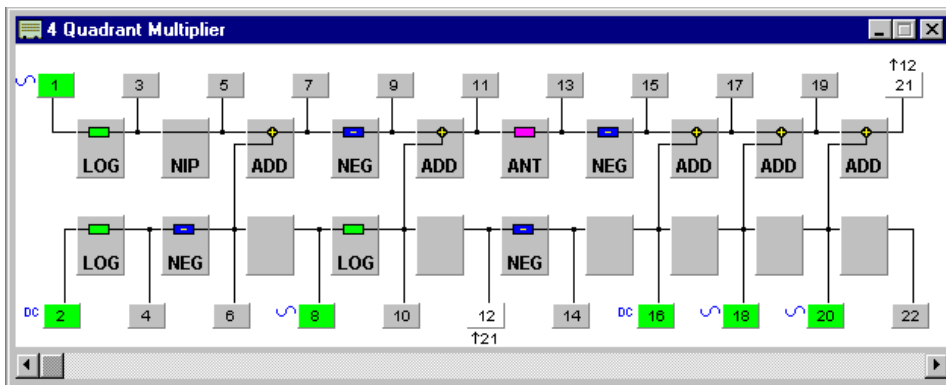


Figure 4
TRAC configured as Four Quadrant Multiplier

Compensation and Practical Tolerances

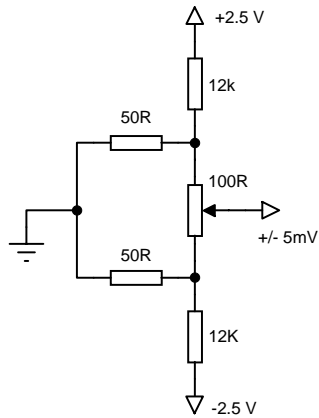


Figure 5
Trimming Circuit

Due to imperfection of all analog devices and components, adjustments have to be made to compensate for all offset voltages and tolerances not accounted for during the design cycle.

In certain Signal Processing applications such as the multiplier, where the accuracy in the processing loop (log domain) is vital for producing the correct result, external compensation must be provided to cancel out all accumulated offsets due to practical tolerances.

Using TRAC, this requirement may be simply accounted for by adding a small DC voltage (around $\pm 5\text{mV}$) to the appropriate node (I/O) in the design.

The Practical Multiplier design outlines the compensation scheme necessary for nulling all accumulated offsets just before transferring the result to the linear domain.

Consideration of the design of the Single Quadrant Multiplier shown in Figure 6 and comparing it with the original design (Figure 3) derived directly from the algorithm, highlights the minor alteration recommended for injecting the nulling offset signal in to IO12 as shown in Figure 6.

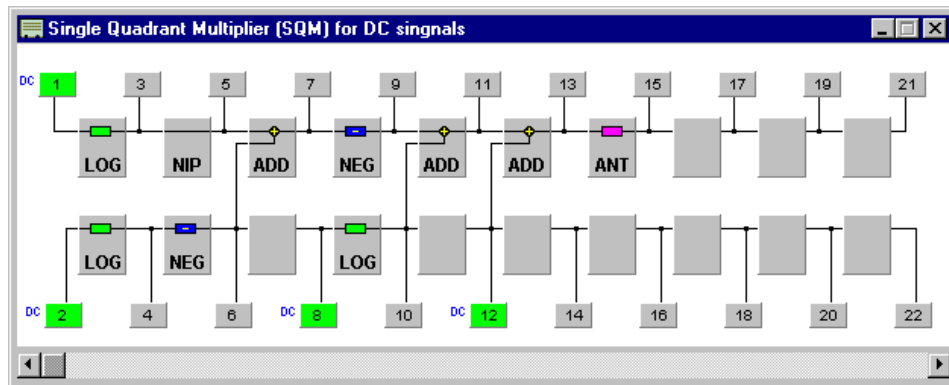


Figure 6
Practical SQM Design Utilising TRAC

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Placing an ADDer before the ANTilog function will provide the required polarity inversion as well as allowing offset compensation to be applied to this section of the design.

Similarly, the design of the four quadrant multiplier (4QM) may be slightly altered by replacing the NEG cell with an ADDer to cater for the offset

nulling requirements as well as providing the required polarity inversion at this node.

The necessary design alteration has been outlined in Figure 7 and the simulation result is outlined in Figure 8.

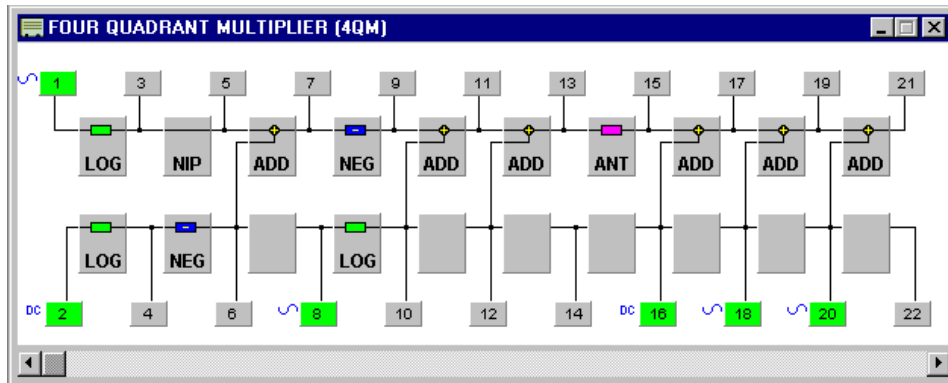


Figure 7
Practical 4QM Design Utilising TRAC

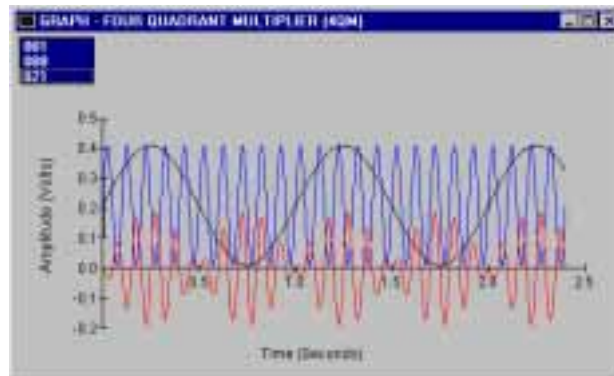


Figure 8
Simulation result for the 4QM design.

TRAC

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