Component Reliability

Introduction

The reliability of Zetex components is rigorously monitored by the use of product qualification and on-going production testing. Testing is not done only to collect data, but this data is used to improve the reliability of future Zetex components.

In this note, the basic theory of reliability testing and failure rate calculations are covered, along with how Zetex carry out component qualification exercises and failure analysis, so as to ensure the on-going improvement of Zetex products.

Reliability Theory

Reliability can be defined as the probability of failure free performance of a required function, under a specified environment, for a given period of time. During this lifetime three distinct phases exist:

a) Infant Mortality:
Occurs in the first few hours of operating life. In this region, there is a high failure rate initially which then falls over the next few hours.

b) Random Failures:
Follows the infant mortality period and occurs over a long period of time. During this period there is a low, almost constant failure rate, with failures occurring due to random effects.

c) Wear out Region:
During this phase the number of failures begins to rise again as a result of devices reaching the end of their useful life.

A graphical representation of these three phases is shown in figure 1. This curve is frequently referred to as the "bath tub" curve.

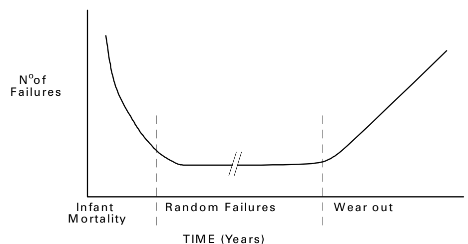

Figure 1.
Number of Failures with time.

Calculation of Failure Rate

Numerous concepts and mathematical models have been proposed to assess the reliability performance of semiconductor components. In this section, two parameters will be considered; thermal activation energy and failure rate.

Thermal Activation Energy

The thermal activation energy is used in determining the acceleration factor for a particular test when related to a lower standard operating temperature. The thermal activation energy can be determined for each failure mechanism and then substituted into the Arrhenius equation so as to calculate the thermal acceleration factor.

$$\text{Acceleration factor} = \exp[Ea/K(T_1^{-1} - T_2^{-1})]$$

where:

T_1 = Test temperature in degrees K.
T_2 = Standard operating temperature in degrees K.
K= Boltzmans constant.
Ea = Activation energy.

This factor can then be used in the failure rate calculation.

Failure Rate

Failure rates can be calculated by using the average failure rate calculation. This equation makes use of the “bath-tub” curve where the random region is assumed to be constant. Appropriate junction temperatures and thermal acceleration factors are used in the calculation along with a confidence limit (usually 60%) for the activation energy. The failure rate for a particular device is then calculated as:

$$\text{Failure Rate} = \frac{K(n) \times 10^9}{H}$$

where:
K(n) = Factor dependant upon total number of failures and the upper confidence limit chosen.
H = Equivalent number of device hours on test (i.e. utilising the acceleration factor calculated) to accumulate “n” failures.

The failure rate is thus quoted in FIT’s with 1 FIT (Failure In Time) equating to 1 failure per billion hours of operation.

NOTE: FIT calculations for generic Zetex product (by package style) are included in appendix A.

Product Qualification

Qualification Tests

All new Zetex products and process changes are qualified using accelerated test methods, to ensure that the design or process change is reliable. These accelerated tests are used to model actual service conditions through increased temperatures, humidities, voltages etc. The following sections summarise these tests:

a) High Temperature Reverse Bias (HTRB)
The HTRB test is used to accelerate failure mechanisms which are thermally activated through the application of extreme temperatures and the use of

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biased operating conditions. The temperature and voltage conditions used in the stress will vary with the product being tested.

b)Electrical Endurance and Power Cycling
These tests are performed to assess the quality of die attach and wire bond processes and is carried out with the product operating at maximum power, (with electrical endurance tests) and intermittent maximum power (for power cycling tests).

c) Humidity Tests
Three humidity tests are performed: (i) Temperature Humidity bias, (ii) Damp heat cyclic and (iii) Autoclave. In the temperature humidity bias test, an environment of 85°C, 85% relative humidity is established. The test is designed to measure the moisture resistance of plastic encapsulated devices. A reverse bias is applied to the device to create electrolytic cells which can then accelerate corrosion of the aluminium metalisation, if contamination is present.

The cyclic damp heat test is designed to examine the combined effects of temperature cycling, high humidity and temperature. This test is performed un-biased and uses an environment of 55°C and 95% relative humidity.

The autoclave test uses an environment of 121°C, 100% relative humidity and 15 psi. These conditions are used to test the devices' resistance to moisture penetration and the resultant effects of corrosion.

d) High Temperature Storage
This test is used to measure the stability of packaged devices to long term, un-biased storage. Typical failure mechanisms that will be accelerated by this test are die attach and wire bond related faults.

e) Temperature Cycling
Three temperature cycling tests are performed; (i) temperature cycling, (ii) thermal shock, (iii) resistance to solder heat.

With temperature cycling, the devices are cycled from -55°C to +150°C in an air environment with a total cycle from cold to hot taking one hour. This test is designed to accelerate the effects of thermal mis-match amongst the die/assembly components.

The objective of thermal shock testing are the same as that for temperature cycling. However, thermal shock presents additional stress conditions in that the device is exposed to a sudden temperature change created by the use of a liquid ambient.

The resistance to solder heat test is used to establish the devices' ability to withstand the temperatures seen during a board soldering process.

Qualification Programs

In order that products and process are designed in such a way as to ensure that reliable product is manufactured, new products and processes are thoroughly tested against a variety of the tests described in the previous section. Once released to the production departments, these products and processes are then

continually assessed via the Zetex Reliability Monitor Program. This monitor program is designed to:

a) Provide a periodic evaluation of all products (see note below) on an on-going basis and,

b) To aid in the development of new products by establishing the current limitations.

NOTE 1: In order to ensure that a representative range of products are tested, the monitor program looks at all package styles on a monthly basis and product families on an annual basis, with the rate of testing commensurate with the volume of a particular product family being manufactured by the manufacturing group.

NOTE 2: Reliability data can be requested at any time from Zetex. MTBF and FIT values can be calculated for all package styles and for most product types. However, should only limited data be available for a specific product, generic calculations can be provided.

Failure Analysis

The primary purposes of failure analysis are:

1. To close the loop between the customer and Zetex for customer returned parts.

2. To determine the cause for device malfunction and parametric degradation.

3. To provide data for the continuous improvement in the reliability of Zetex products and processes. Material and failure analysis forms an important part of Zetex's commitment to product and process improvement. Results of all analyses are fed back into the development stage of new products, thus ensuring a continuing improvement in product reliability.

Failure analysis of all devices follows a systematic flow which leads to determining the root cause of failure. This analysis flow, along with some of the associated analytical steps is shown in figure 2.

Once a failure mechanism has been identified, the results are recorded and action taken to eliminate the cause in future by means of an improvement or corrective action team.

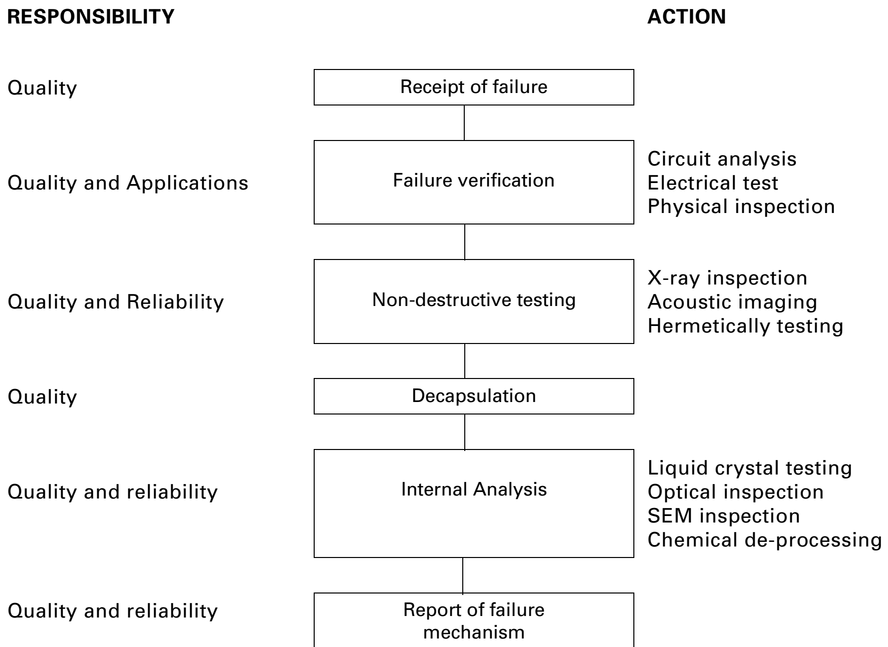

Figure 2
Failure Analysis Flowchart.

Appendix A

E-LINE PACKAGE: HIGH TEMPERATURE REVERSE BIAS

V_{CB}=80%$V_{CB(MAX)}$; T_A=200°C

PRODUCT	NO. OF LOTS	DEVICES TESTED	CUM.DEV CYCLES	EQUIV.DEV. CYCLES	NO. OF REJECTS	T_a = 90°C FIT RATE 60% CL
SMALL SIGNAL NPN	7	168	61504	1.644E+08	1	12.29
PNP	8	176	62848	1.866E+08	0	4.93
SUPER E-LINE NPN	5	300	133600	1.065E+08	3	39.24
PNP	5	250	216800	1.729E+08	8	54.67
MED POWER NPN	3	60	43360	1.288E+08	0	7.15
PNP	2	40	23360	6.937E+07	0	13.26
NMOS	2	100	16800	9.888E+05	0	930.45
PMOS	1	50	8400	4.944E+05	0	1860.91
NPN HV	3	200	125200	9.982E+07	2	31.16
PNP HV	1	50	8400	6.697E+06	1	301.61
TOTAL E - LINE	39	1420	701104	9.39E+08	16	18.74

SOT-23 PACKAGE: HIGH TEMPERATURE REVERSE BIAS

V_{CB}=80%$V_{CB(MAX)}$; T_A=150°C

PRODUCT	NO. OF LOTS	DEVICES TESTED	CUM.DEV CYCLES	EQUIV.DEV. CYCLES	NO. OF REJECTS	T_a = 90°C FIT RATE 60% CL
NPN SMALLSIGNAL	1	38	38000	8.853E+06	0	103.93
MED POWER	1	38	38000	8.853E+06	1	228.18
NPN SWITCH	2	115	50936	9.614E+06	2	323.49
NPN SUPERSOT	1	50	8400	4.944E+05	0	1860.91
PNP SUPERSOT	1	77	77000	4.597E+06	0	197.9
NMOS	7	484	324432	6.140E+06	2	162.87
PMOS	1	50	8400	4.944E+05	0	1860.91
NPN HV	5	238	71600	1.083E+07	6	678.67
PNP HV	5	341	193736	1.802E+07	1	112.11
ZENER DIODES	2	79	76000	1.771E+07	0	51.96
SWITCH DIODES	4	195	68536	1.339E+07	0	69.7
TOTAL SOT-23	30	1675	886440	1.078E+08	12	126.11

SOT-223 PACKAGE: HIGH TEMPERATURE REVERSE BIAS

V_{CB}=80% $V_{CB(MAX)}$; T_A=+150°C

PRODUCT	NO. OF LOTS	DEVICES TESTED	CUM.DEV CYCLES	EQUIV.DEV CYCLES	NO. OF REJECTS	T_a = 90°C FIT RATE 60% CL
NPN SWITCH	1	50	8400	4.944E+05	0	1860.91
NPN SUPER SOT223	3	150	116800	6.874E+06	1	293.85
PNP SUPER SOT223	5	300	183600	1.081E+07	1	186.94
NPN MED POWER	1	50	8400	4.944E+05	0	1860.91
NPN HV	2	100	108400	6.38E+06	0	144.2
NMOS	4	250	125200	7.369E+06	3	567.27
TOTAL SOT 223	16	900	550800	3.242E+07	5	194.34

SOT-223 PACKAGE : ELECTRICAL ENDURANCE

T_A =+25°C, V_{CE} = 100% RATED V_{CE}: PD = MAX RATED POWER

PRODUCT	NO. OF LOTS	DEVICES TESTED	CUM.DEV CYCLES	EQUIV.DEV CYCLES	NO. OF REJECTS	T_a = 60°C FIT RATE 60% CL
NPN SWITCH	2	150	116800	9.695E+07	2	32.08
NPN SUPER SOT223	5	300	183600	1.145E+07	0	80.33
PNP SUPER SOT223	3	150	116800	9.695E+07	0	9.49
NPN MED POWER	2	100	58400	4.847E+07	0	18.98
PNP MED POWER	3	150	25200	1.572E+06	2	1978.44
NPN HV	1	50	8400	5.240E+05	4	10019.43
PNP HV	1	75	48376	1.014E+06	0	907.2
NMOS	1	50	50000	3.119E+06	0	294.97
TOTAL SOT-223	17	950	559200	4.641E+08	8	20.36

ELECTRICAL ENDURANCE : E-LINE PACKAGE

T_A = +25°C, V_{CE} = 100% RATED V_{CE}: PD = MAX RATED POWER

PRODUCT	NO. OF LOTS	DEVICES TESTED	CUM.DEV CYCLES	EQUIV.DEV. CYCLES	NO. OF REJECTS	T_a = 60°C FIT RATE 60% CL
SMALL SIGNAL NPN	27	2766	572016	9.155E+07	7	91.75
PNP	20	1605	305416	6.991E+06	6	1051.4
NPN SWITCH	2	118	91376	3.376E+05	0	2725.4
PNP SWITCH	4	225	145128	7.238E+06	0	127.1
SUPER E - LINE NPN	6	375	261928	2.607E+09	0	0.35
PNP	7	374	139376	1.284E+09	2	2.42
MED POWER NPN	13	964	275104	1.378E+09	3	3.03
PNP	5	340	148720	1.014E+09	1	1.99
NMOS	9	478	223408	1.111E+08	0	9.00
PMOS	2	175	106776	6.804E+07	0	13.52
NPN HV	4	290	48720	8.926E+07	0	10.31
SCHOTTKY DIODE	1	93	51400	9.152E+04	0	10052.01
TOTAL E - LINE	103	7899	2385496	6.663E+09	19	3.12

ELECTRICAL ENDURANCE: SOT-23 PACKAGE

T_A =+25°C, V_{CE} = 100% RATED V_{CE}: PD = MAX RATED POWER

PRODUCT	NO. OF LOTS	DEVICES TESTED	CUM. DEV CYCLES	EQUIV.DEV CYCLES	NO. OF REJECTS	T_a = 60°C FIT RATE 60% CL
SMALL SIGNAL NPN	9	540	355496	3.255E+07	0	28.27
PNP	9	575	275480	2.657E+07	0	34.63
NPN SWITCH	9	590	352144	2.310E+07	1	87.46
PNP SWITCH	4	222	100528	7.514E+06	3	556.31
SUPER SOT NPN	2	100	16800	1.316E+07	0	69.93
PNP	1	50	8400	6.578E+06	4	798.08
MED POWER NPN	6	365	174472	7.680E+07	0	11.98
PNP	8	531	322248	2.160E+08	0	4.26
NPN HV	2	113	54760	4.092E+06	0	224.78
PNP HV	4	201	69544	1.115E+07	0	82.52
ZENER DIODE	20	1353	1355160	1.094E+07	1	184.55
SWITCH DIODE	18	924	401504	3.723E+06	2	268.21
TOTAL SOT-23	93	5614	3494936	4.401E+08	11	28.63

PACKAGE INTEGRITY TEST RESULTS

HIGH TEMPERATURE/HIGH HUMIDITY

PACKAGE	NO. TESTED	CUMULATIVE DEVICE HOURS	FAIL	% FAIL
E-LINE	899	4.08E+05	2	0.22%
SOT-23	1749	6.43E+05	7	0.4%
SOT-223	1049	4.75E + 05	18	1.72%

TEMPERATURE CYCLING

PACKAGE	NO. TESTED	CUMULATIVE DEVICE CYCLES	FAIL	% FAIL
E-LINE	800	2.59E+05	4	0.5%
SOT-23	1151	5.42E+05	2	0.17%
SOT-223	950	5.59E+05	6	0.63%

THERMAL SHOCK

PACKAGE	NO. TESTED	CUMULATIVE DEVICE CYCLES	FAIL	%FAIL
E-LINE	1976	7.90E+05	0	0.0%
SOT-23	113	4.52E+04	0	0.0%

HOT STORAGE

PACKAGE	NO. TESTED	CUMULATIVE DEVICE CYCLES	FAIL	%FAIL
E-LINE	1681	1.68E+06	2	0.12%
SOT-23	1488	1.48E+05	0	0.0%

RESISTANCE TO SOLDER HEAT

PACKAGE	NO. TESTED	CUMULATIVE DEVICE CYCLES	FAIL	%FAIL
E-LINE	342	N/A	0	0.0%
SOT-23	890	N/A	0	0.0%